

# ECC on small devices

Junfeng Fan

Katholieke Universiteit Leuven, Belgium

[junfeng.fan@esat.kuleuven.be](mailto:junfeng.fan@esat.kuleuven.be)



- What is a small device?

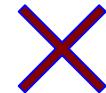
➤ What is a small device?



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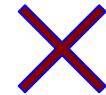


Trusted Platform Module

➤ What is a small device?



Credit Card



Trusted Platform Module

➤ What is a small device?



RFID Tag



Credit Card



Trusted Platform Module



- Why do we want ECC on small devices?



RFID Tag



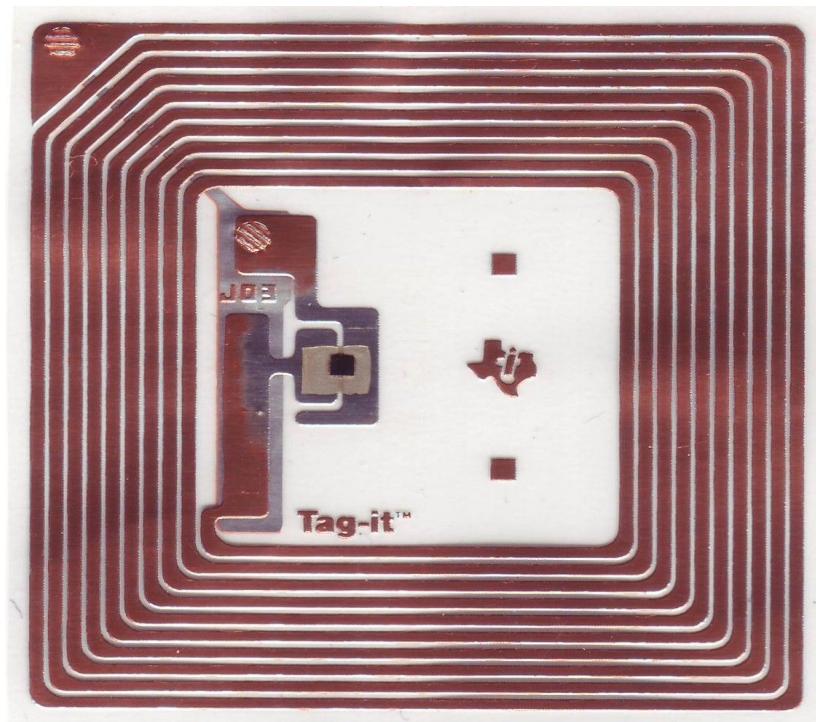
Credit Card



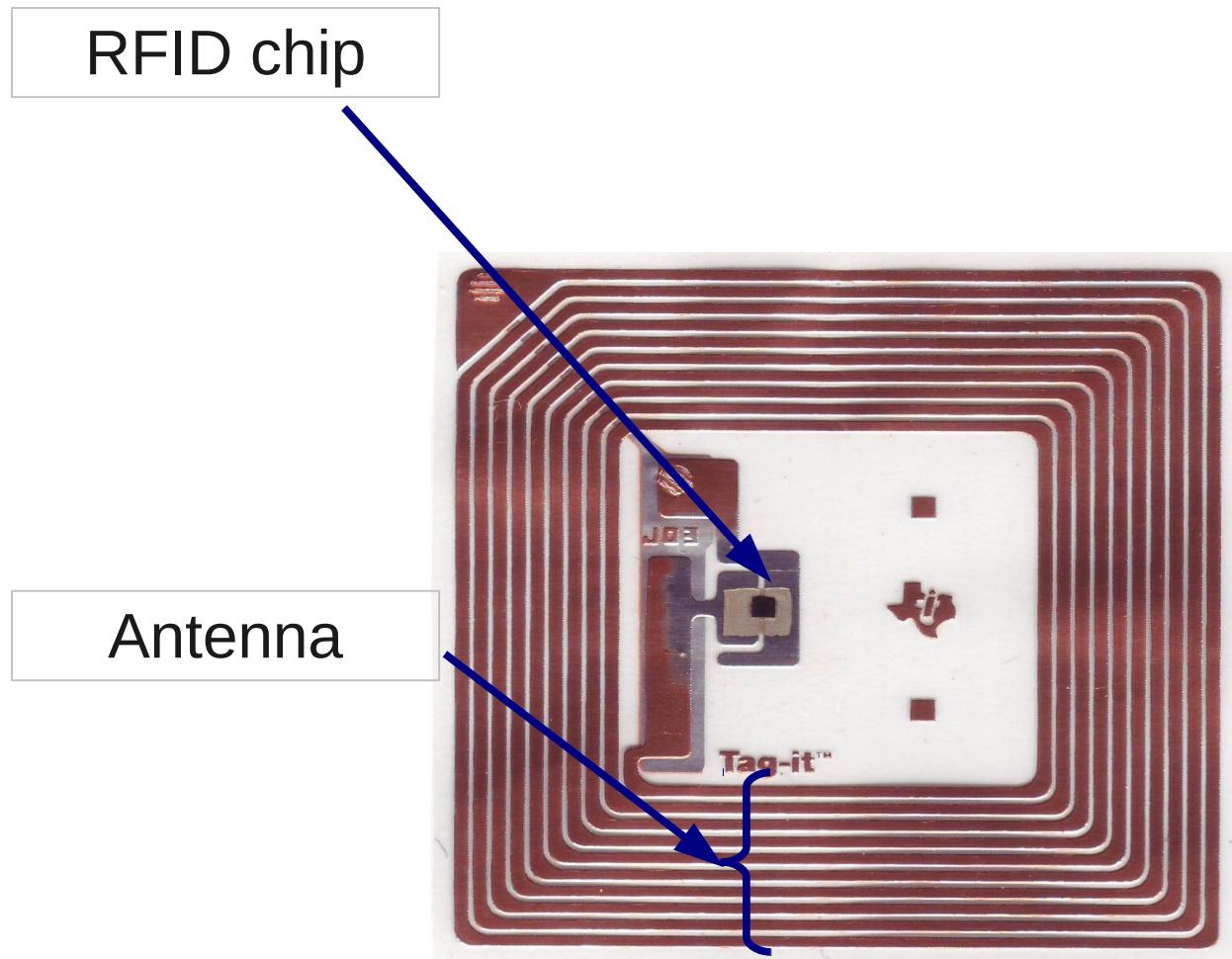
Trusted Platform Module



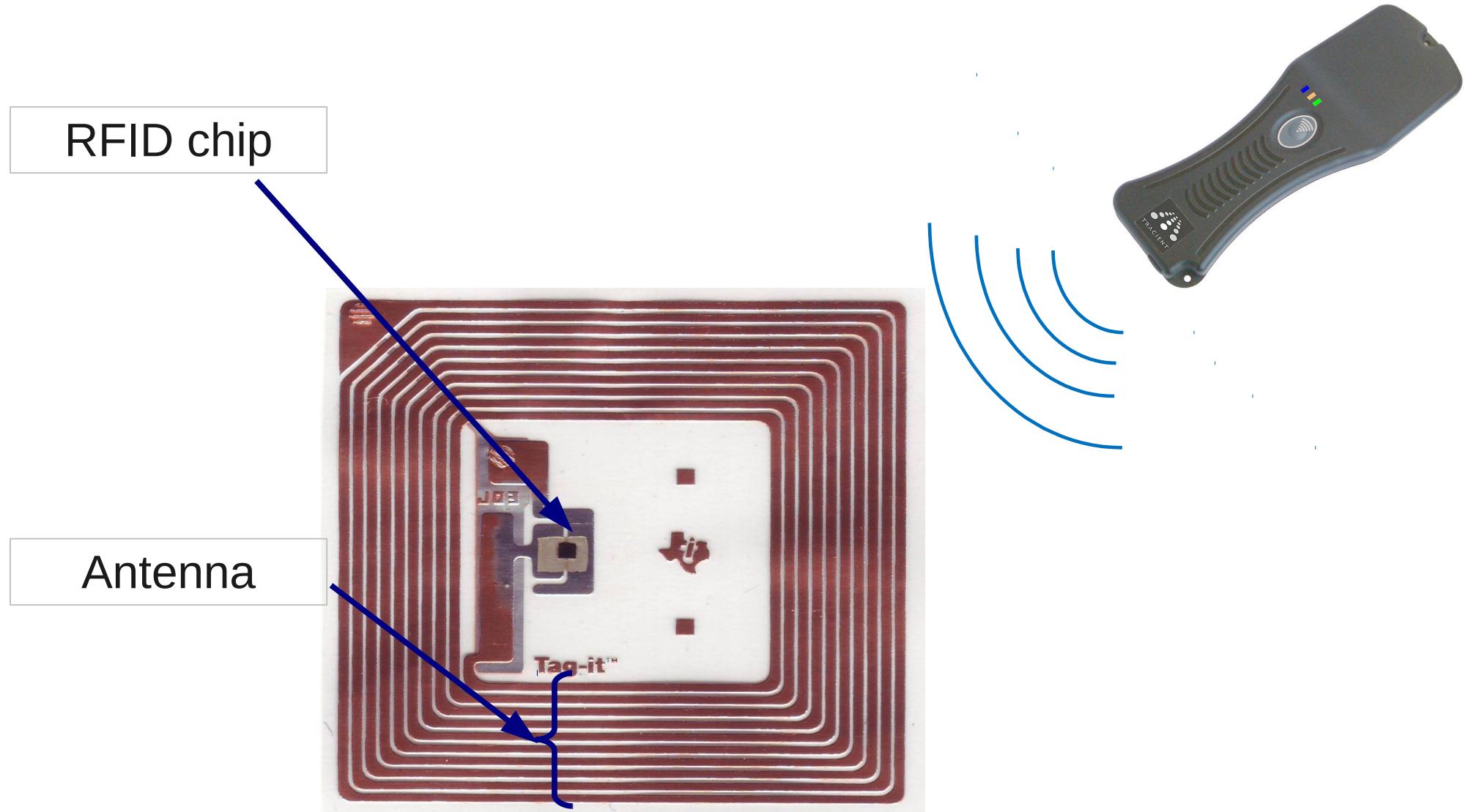
- Let's take RFID as an example...



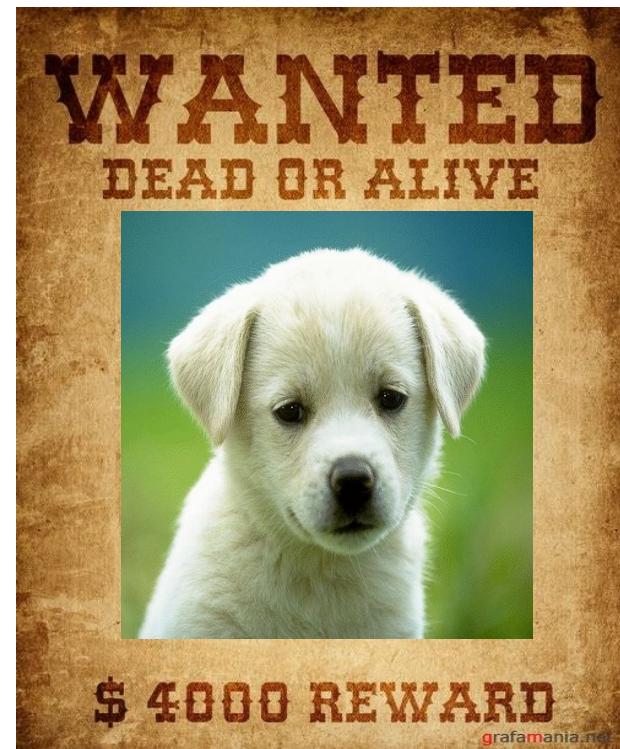
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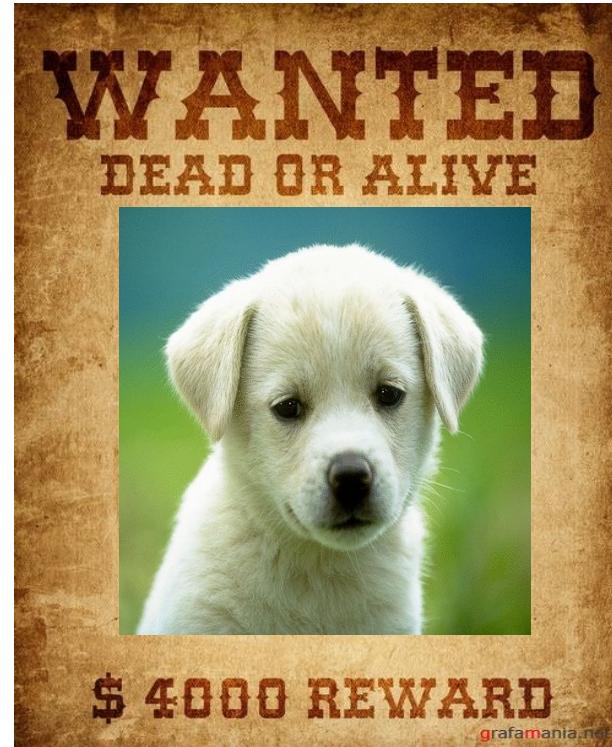


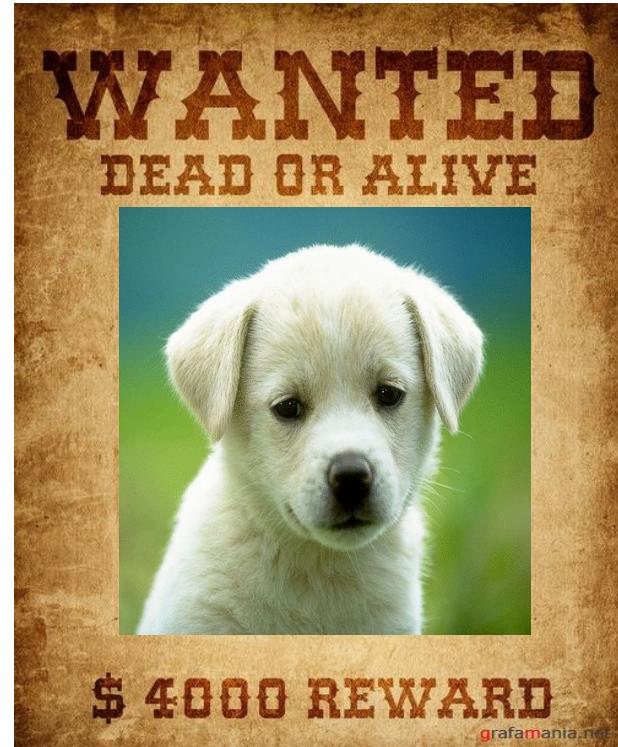
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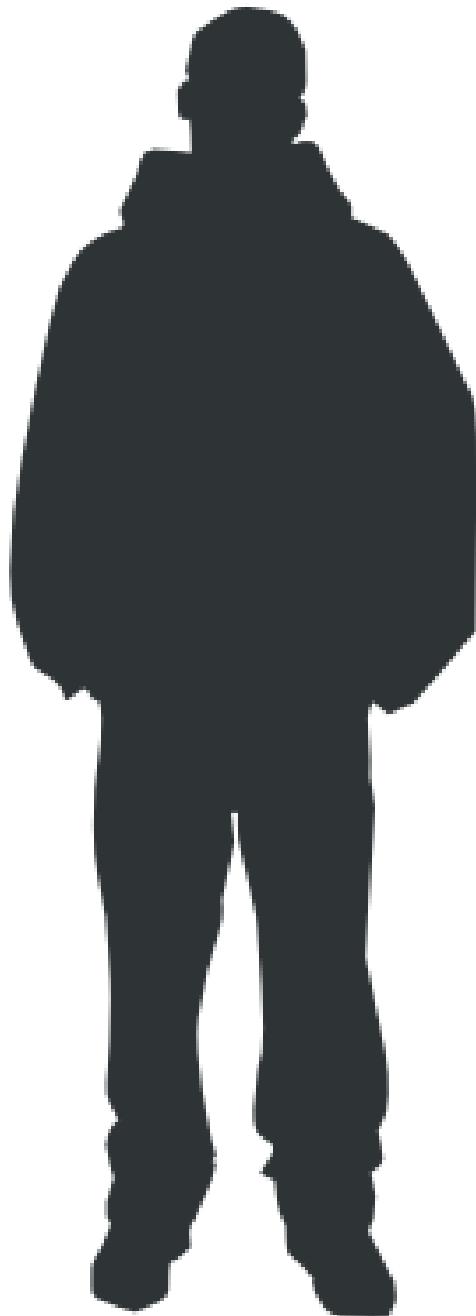






- The problem is....privacy.

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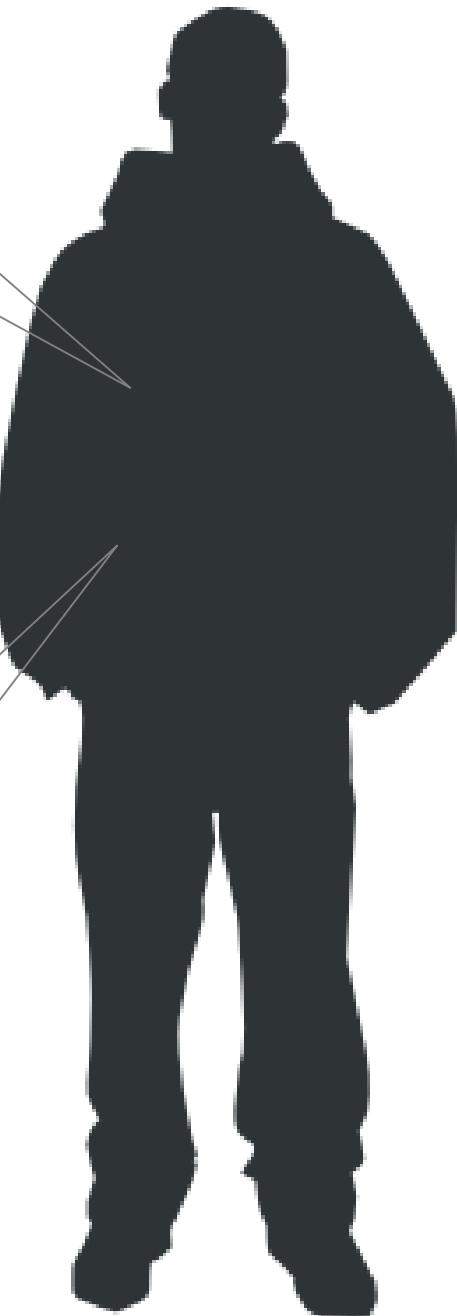


- The problem is....privacy.

**ID:**  
**Thomas XXX**  
13.08.1976  
Dengerland

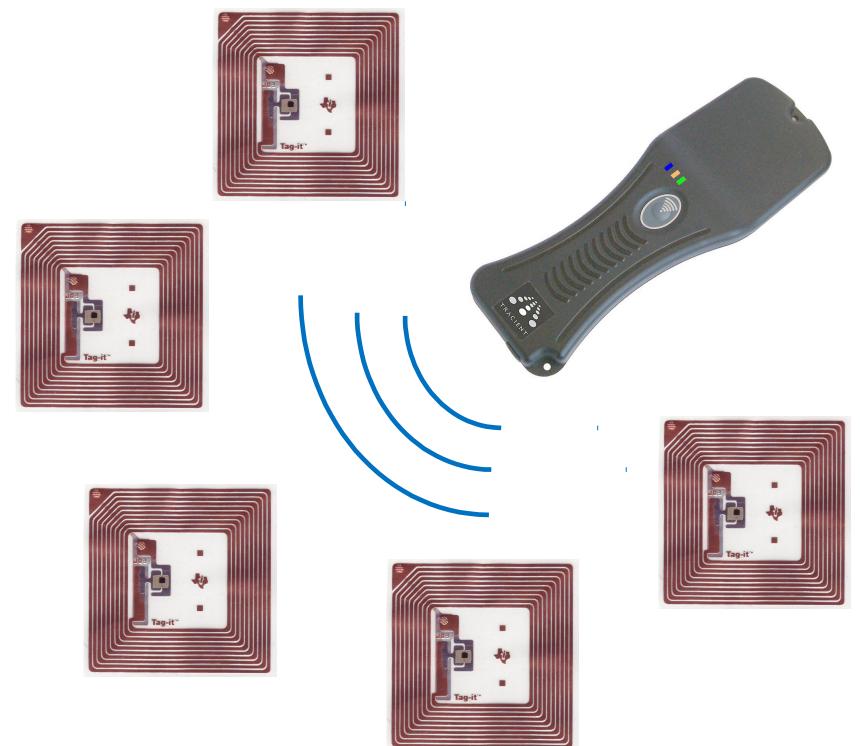


- The problem is....privacy.

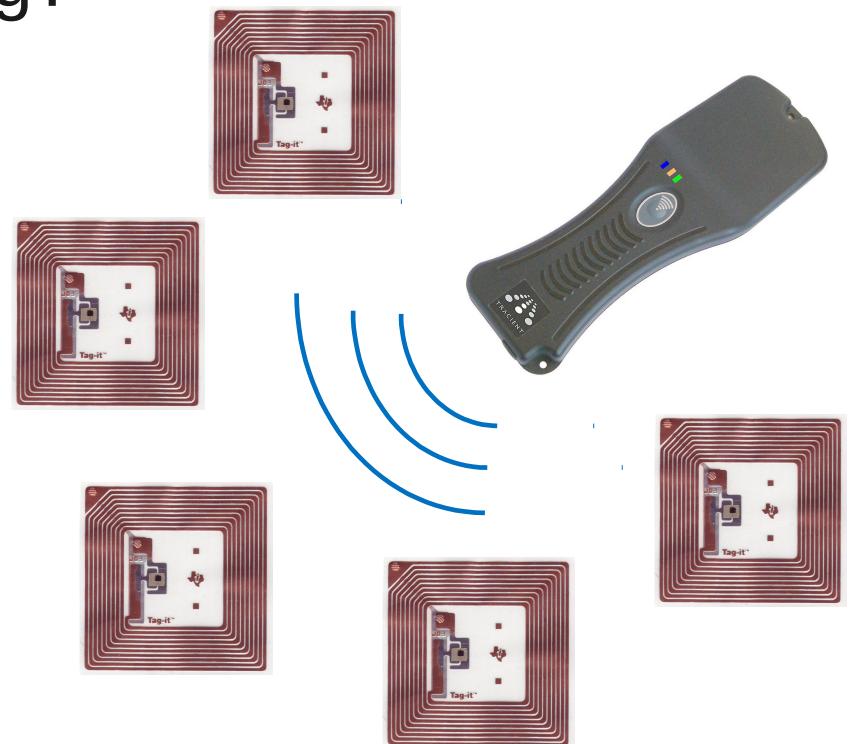


- The problem is....privacy.





- What makes a good RFID tag?



➤ What makes a good RFID tag?



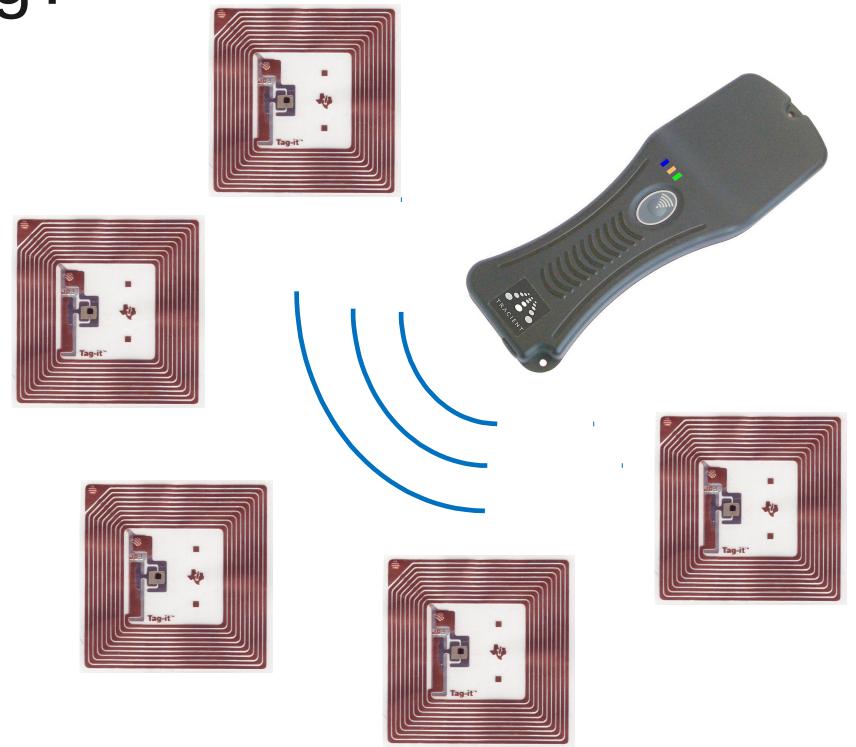
◆ It works!

➤ What makes a good RFID tag?



- ◆ It works!
- ◆ It's cheap.

➤ What makes a good RFID tag?



- ◆ It works!
- ◆ It's cheap.
- ◆ It's secure.

➤ What makes a good RFID tag?



- ◆ It works!
- ◆ It's cheap.
- ◆ It's secure.
- ◆ It's untraceable.

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- ◆ It works!
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Small area



➤ What makes a good RFID tag?



- ◆ It works!
- ◆ It's cheap.
- ◆ It's secure. → Small area
- ◆ It's untraceable.
- ◆ It's scalable.
- ◆ It's fast. → Crypto

➤ What makes a good RFID tag?



- ◆ It works!
  - ◆ It's cheap.
  - ◆ It's secure.
  - ◆ It's untraceable.
  - ◆ It's scalable.
  - ◆ It's fast.
- Small area
- Crypto
- PKC

➤ What makes a good RFID tag?

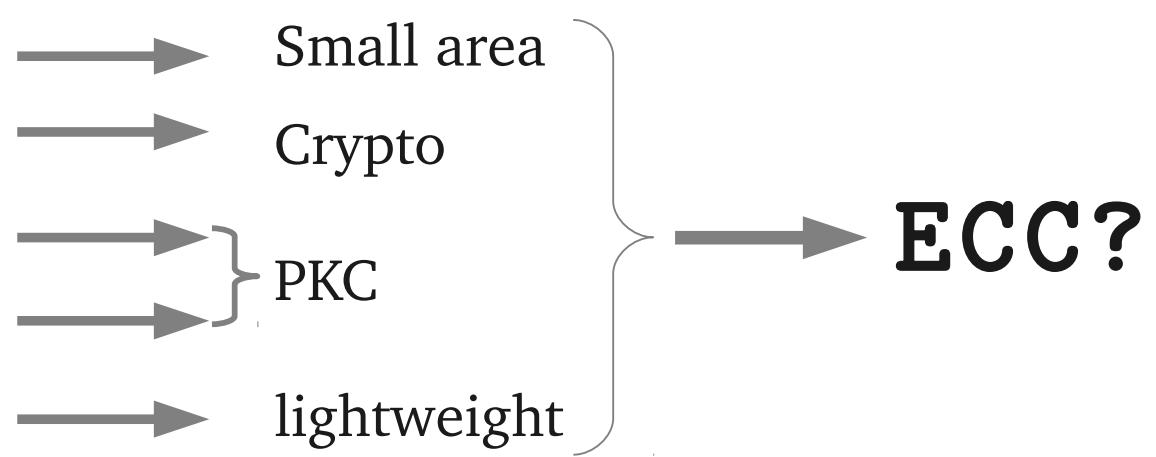


- ◆ It works!
  - ◆ It's cheap.
  - ◆ It's secure.
  - ◆ It's untraceable.
  - ◆ It's scalable.
  - ◆ It's fast.
- Small area
- Crypto
- PKC
- lightweight

➤ What makes a good RFID tag?



- ◆ It works!
- ◆ It's cheap.
- ◆ It's secure.
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- ◆ It's scalable.
- ◆ It's fast.



## ➤ The Schnorr Protocol [Schnorr'89]

- Tag's private key:  $x$
- Tag's public key :  $X(=[-x]P)$

**Reader (Verifier)**

$r_2 = \text{TRNG}()$

If  $[v]P + [r_2]X == R_1$   
Then accept

$R_1$

$r_2$

$v$

**Tag (Prover)**

$r_1 = \text{TRNG}()$

$R_1 = [r_1]P$

$v = xr_2 + r_1 \bmod n$

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**Tag (Prover)**

$r_1 = \text{TRNG}()$

$R_1 = [r_1]P$

$v = xr_2 + r_1 \bmod n$

**Tracing Attack:**  $([v]P - R_1)r_2^{-1} = [x]P = -X$

## ➤ The Vaudenay Protocol [Vaudenay'07]

- Reader's private key :  $K_S, K_M$
- Reader's public key :  $K_P$
- Tag's ID:  $ID$ ,  $K = F_{K_M}(ID)$

**Reader (Verifier)**

$a = \text{TRNG}()$

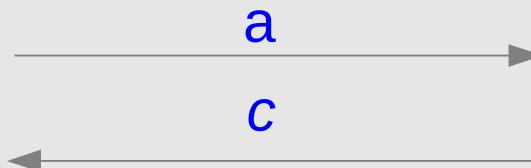
$ID||K||a' = \text{Deck}_S(c)$

If  $a == a'$

$K == F_{K_M}(ID)$

Then accept  $ID$

**Tag (Prover)**



## ➤ The Vaudenay Protocol [Vaudenay'07]

- Reader's private key :  $K_s, K_M$
- Reader's public key :  $K_P$
- Tag's ID:  $ID$ ,  $K = F_{K_M}(ID)$

**Reader (Verifier)**

$a = \text{TRNG}()$

$ID||K||a' = \text{Deck}_s(c)$

If  $a == a'$

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Then accept  $ID$

**Tag (Prover)**

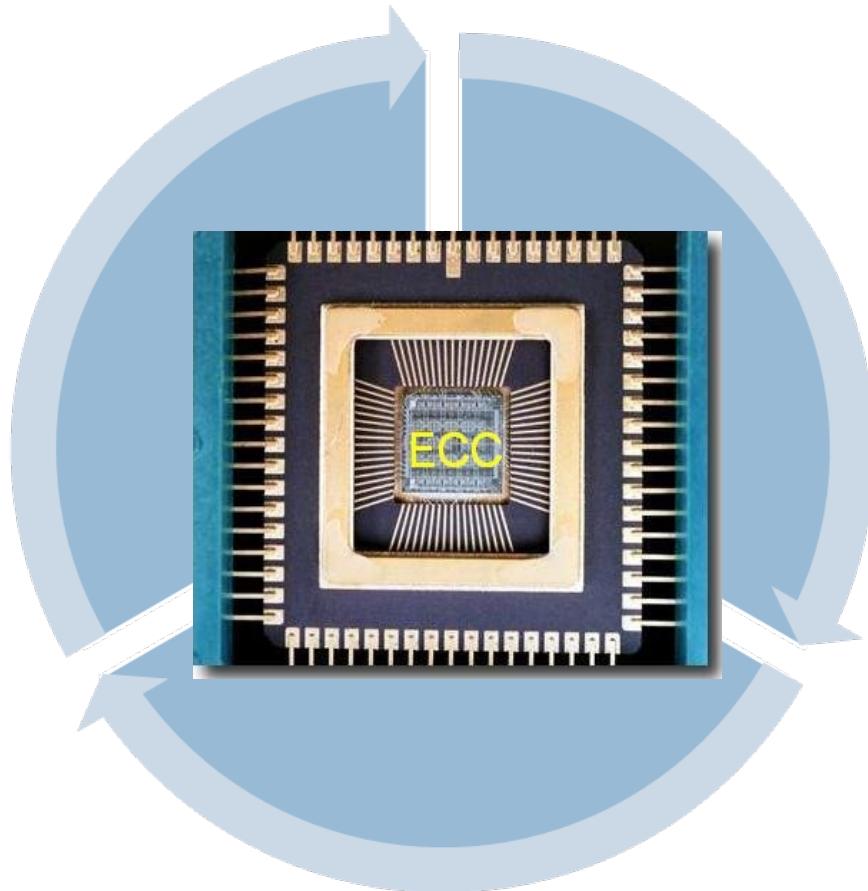
$a$

$c$

$c = \text{Enc}_{K_P}(ID||K||a)$

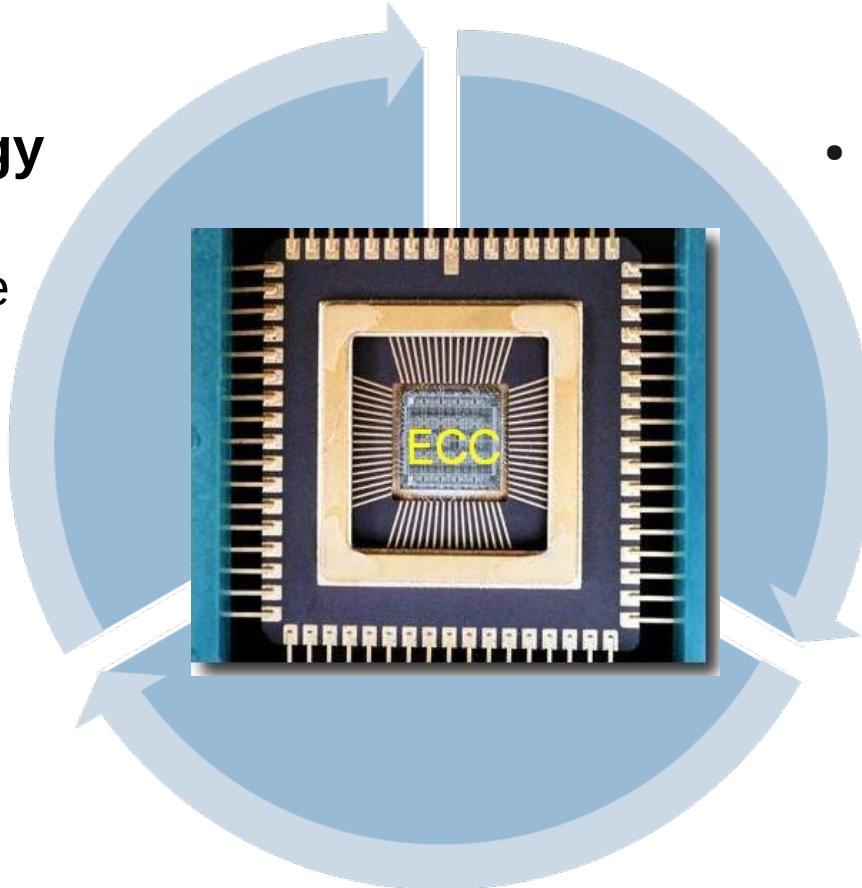
If the PKC in use is **IND-CPA-secure**, then the above RFID scheme is **narrow-strong** private.

- An ECC processor for RFID tags



## ➤ An ECC processor for RFID tags

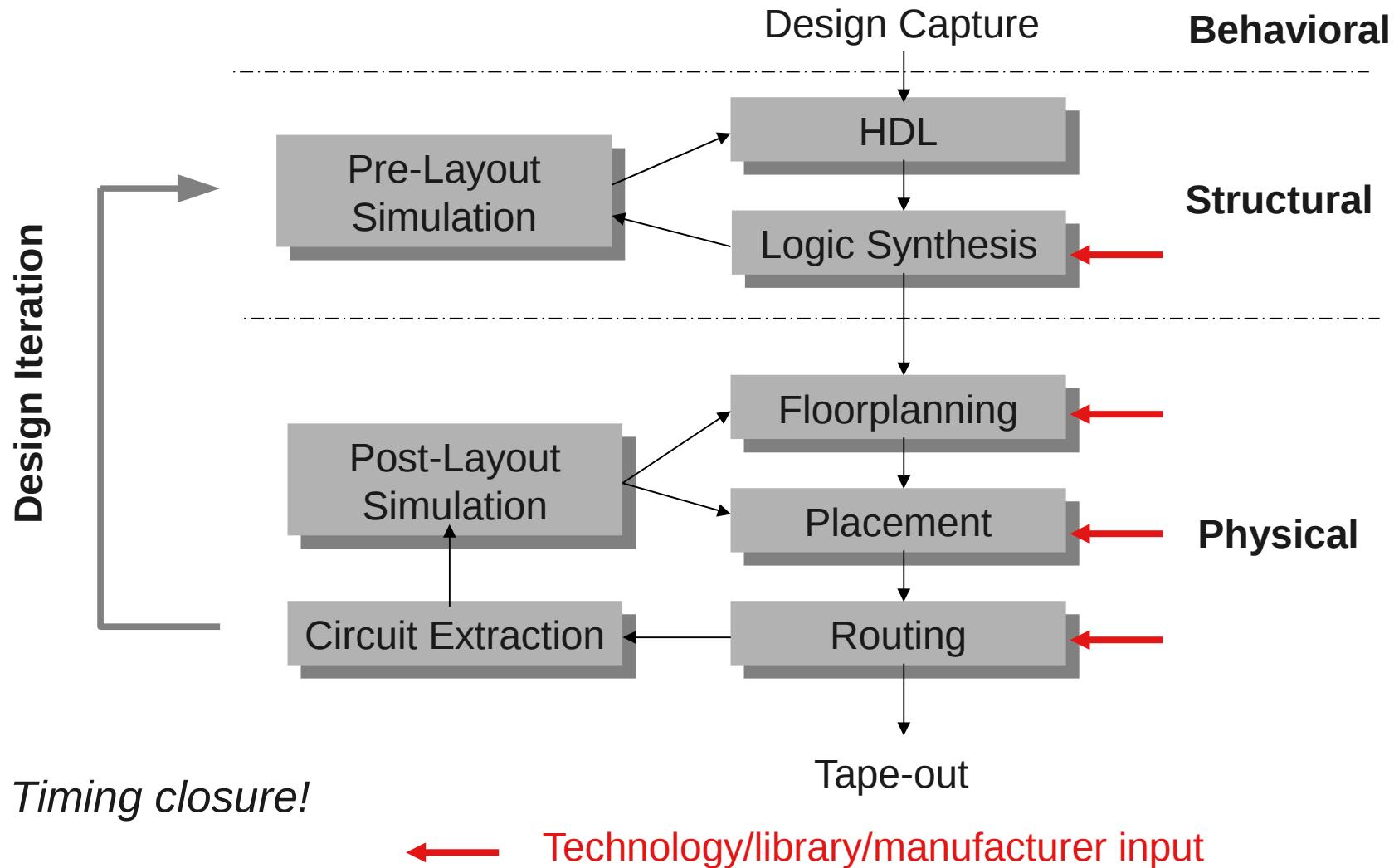
- **Area & Energy**
  - Smaller ALU
  - Less storage



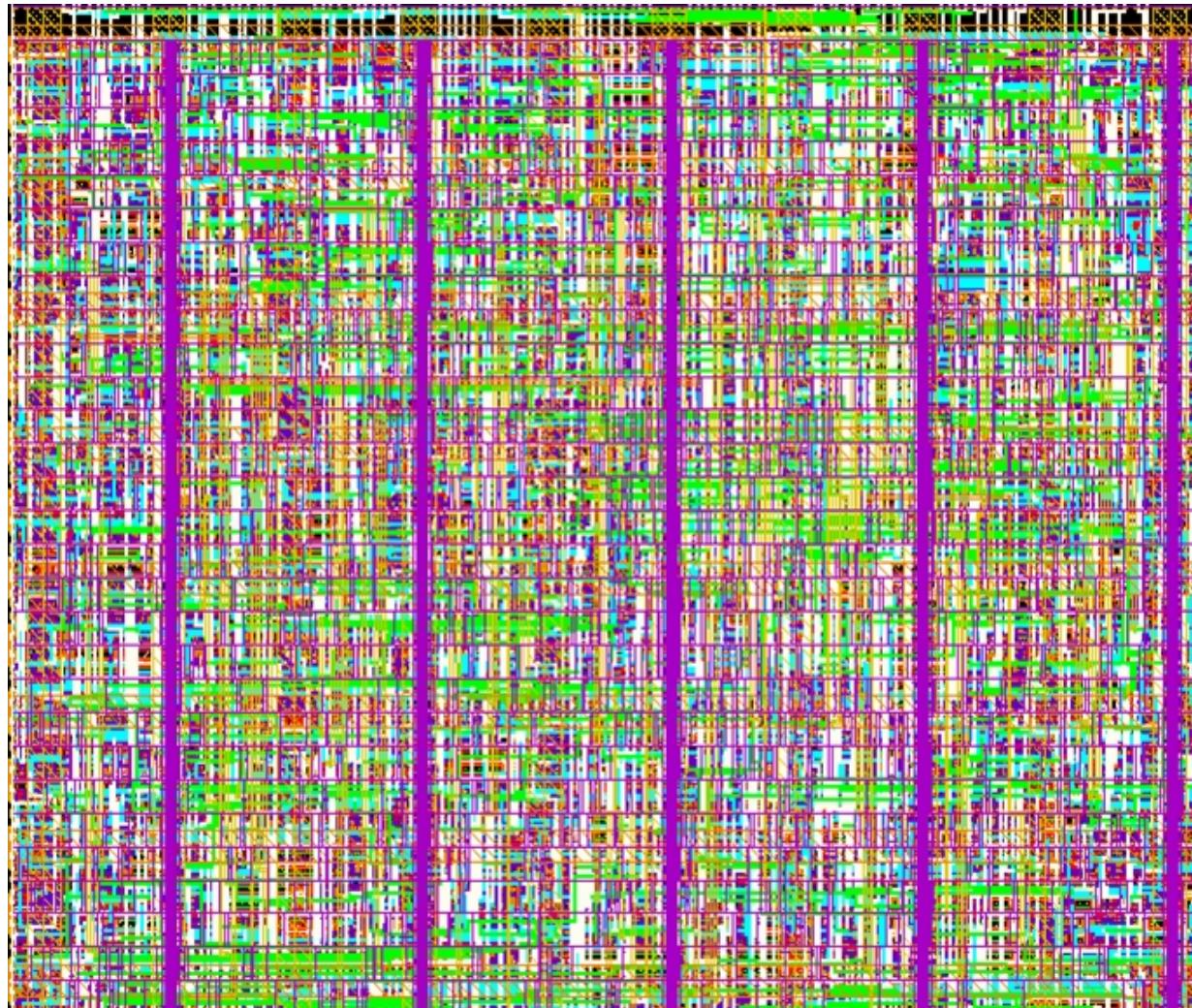
- **Physical Security**
  - Side-channel analysis
  - Fault analysis

- **Performance**
  - Fast field arithmetic
  - Fast group operations

## ➤ Hardware design flow



➤ Layout of an integrated circuit

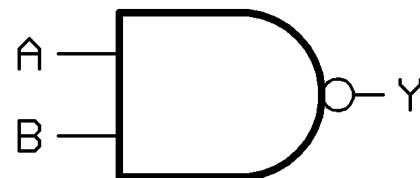


## ➤ Area

- Gate Equivalent (GE): equivalent of NAND gates

## ➤ Area

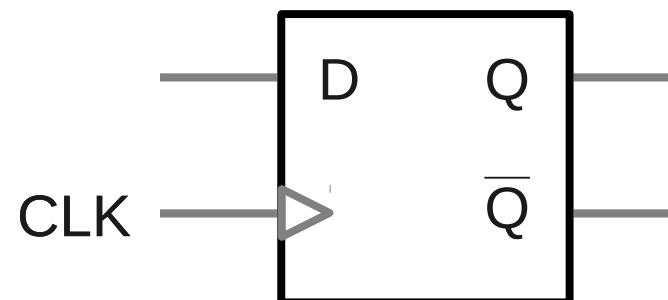
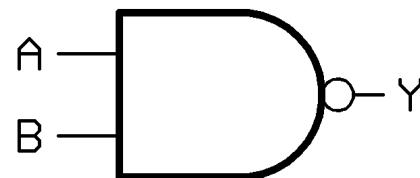
- Gate Equivalent (GE): equivalent of NAND gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

## ➤ Area

- Gate Equivalent (GE): equivalent of NAND gates

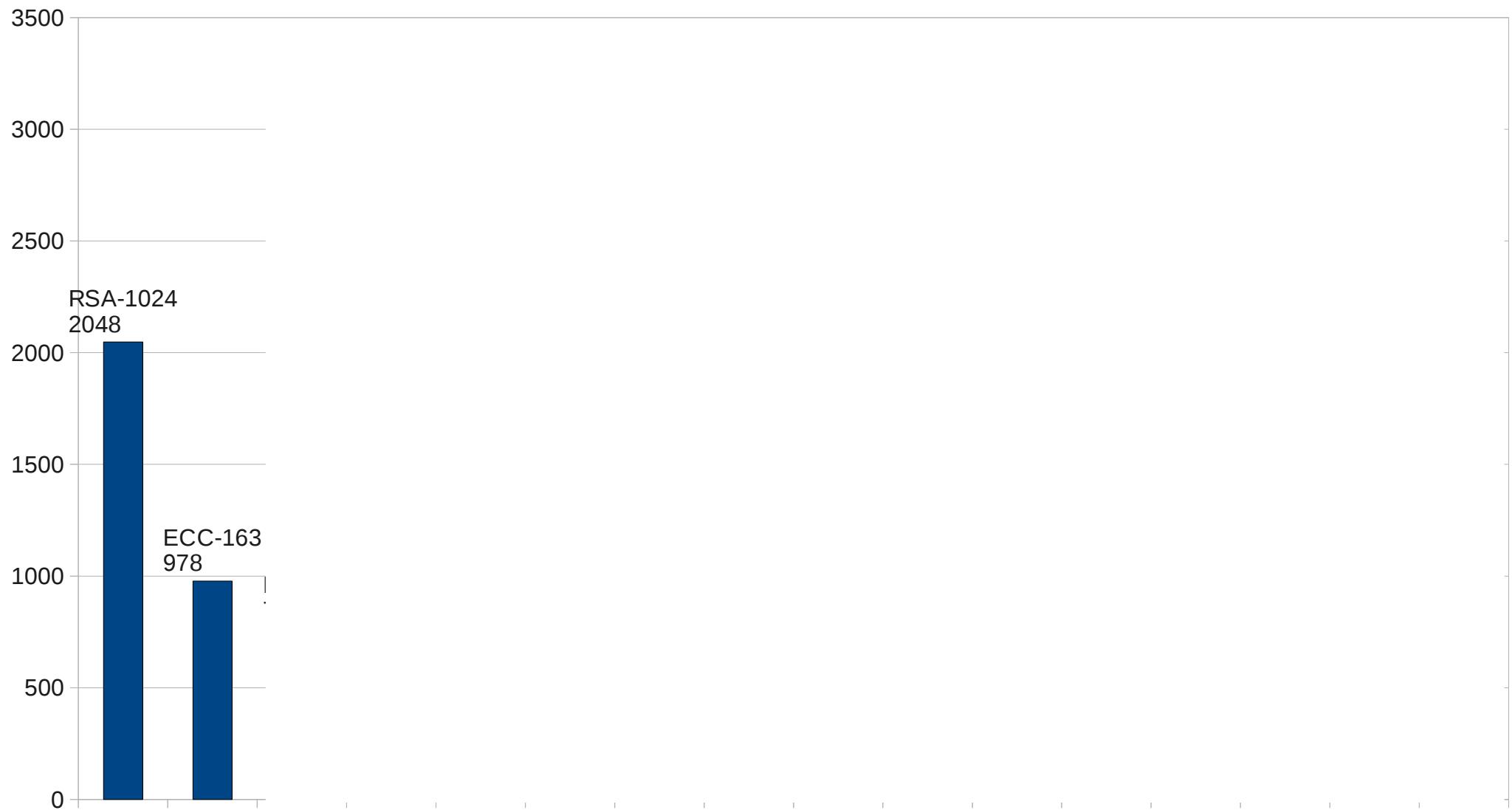


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

D Flip-Flop ( $\approx 6$  GE)

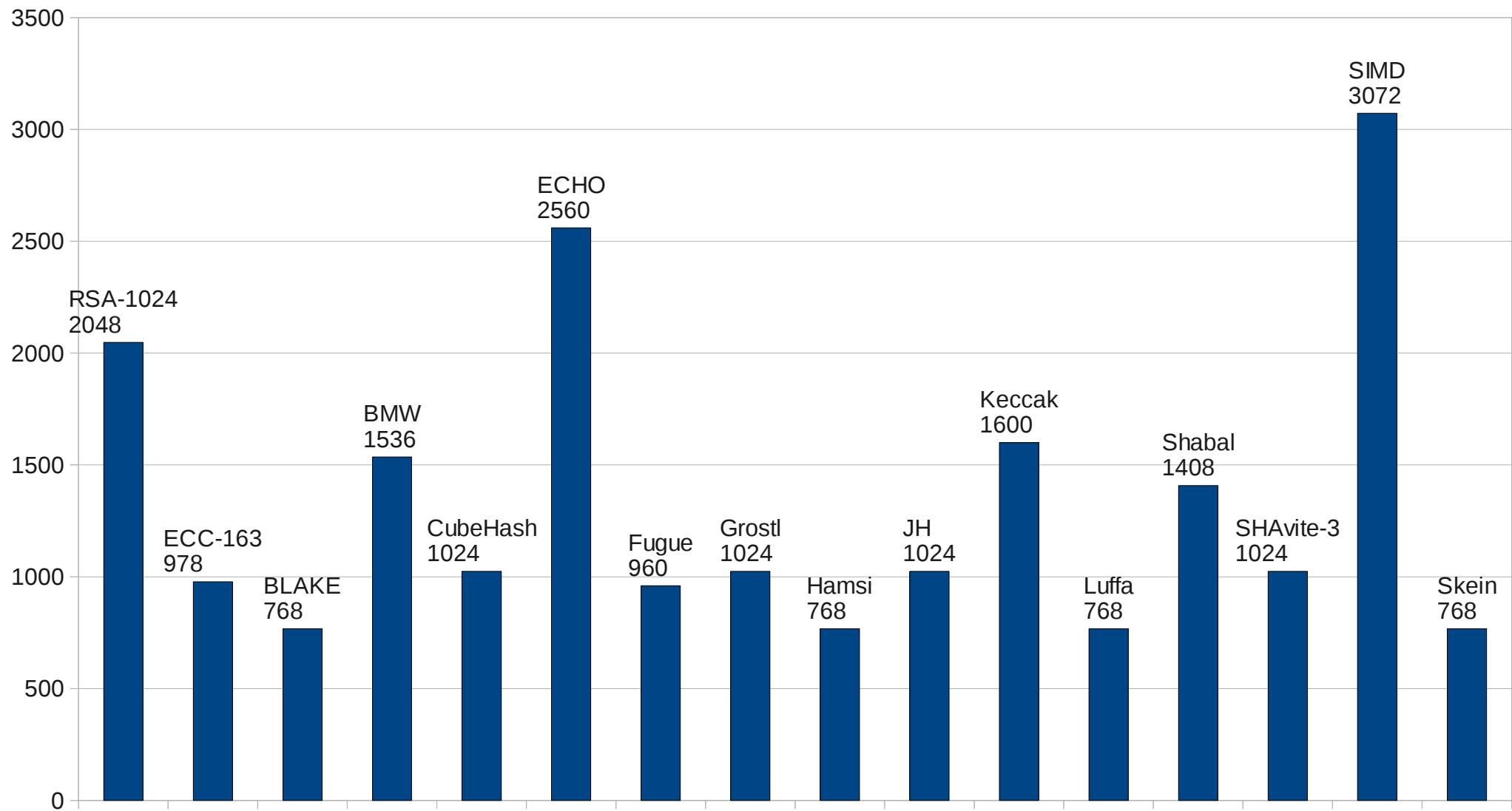
CLK	Q	$\bar{Q}$
	D	$\bar{D}$
	Q	$\bar{Q}$

## ➤ Memory requirement



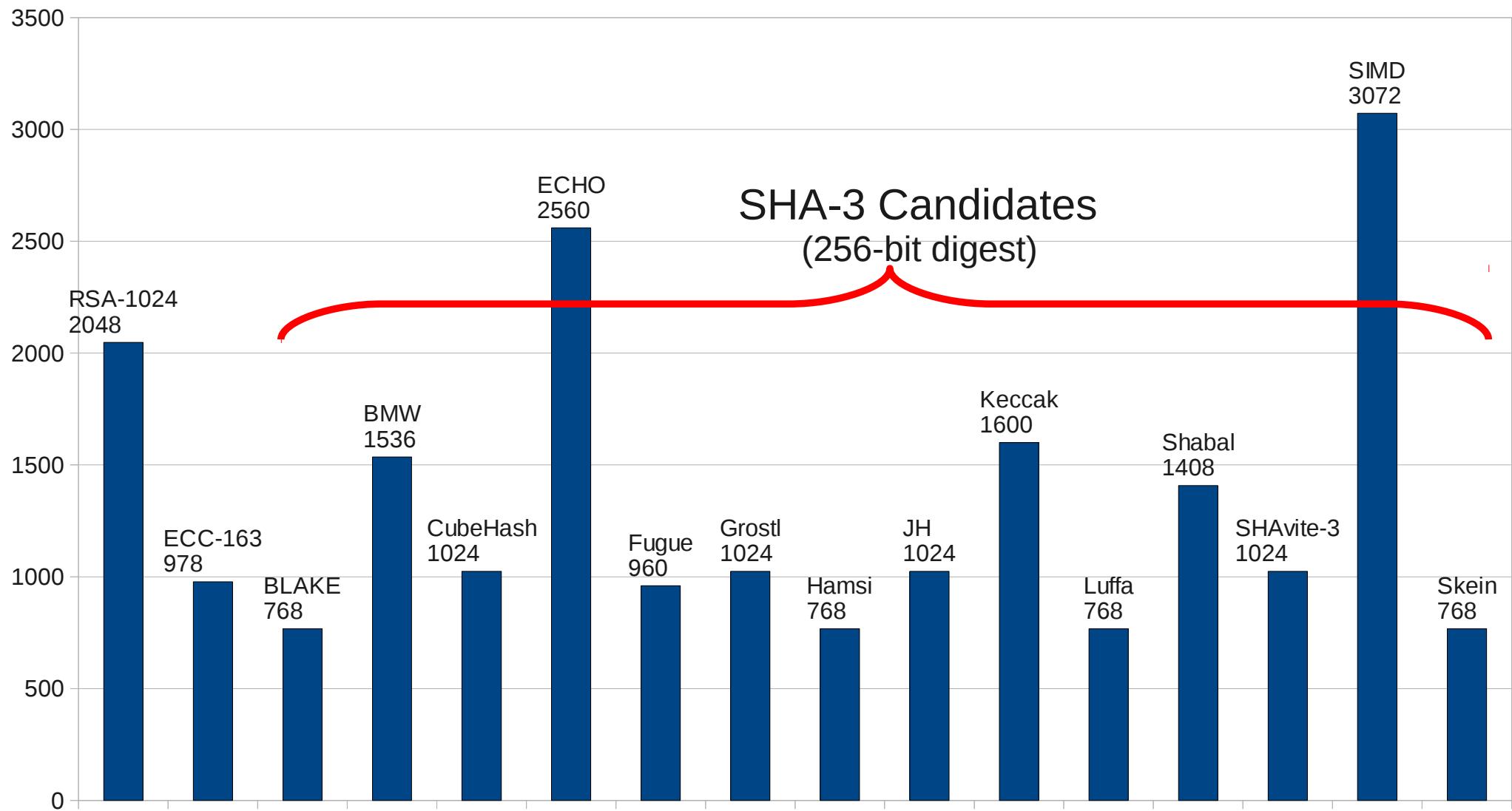
\* Ideguchi *et al*, 2009

## ➤ Memory requirement



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## ➤ Memory requirement



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## ➤ Let's make an ECC processor

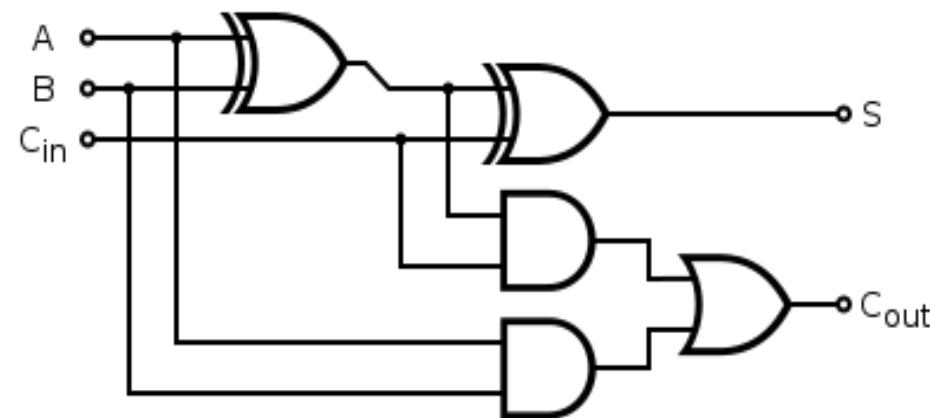
- Binary fields v.s. Prime fields
- Security level
- Coordinate systems
- Representation of field elements
- Architecture
- Physical security properties

## ➤ $\mathbf{F}_{2^m}$ V.S. $\mathbf{F}_p$

- Use binary fields instead of prime fields
  - No carry bits, smaller and faster ALU

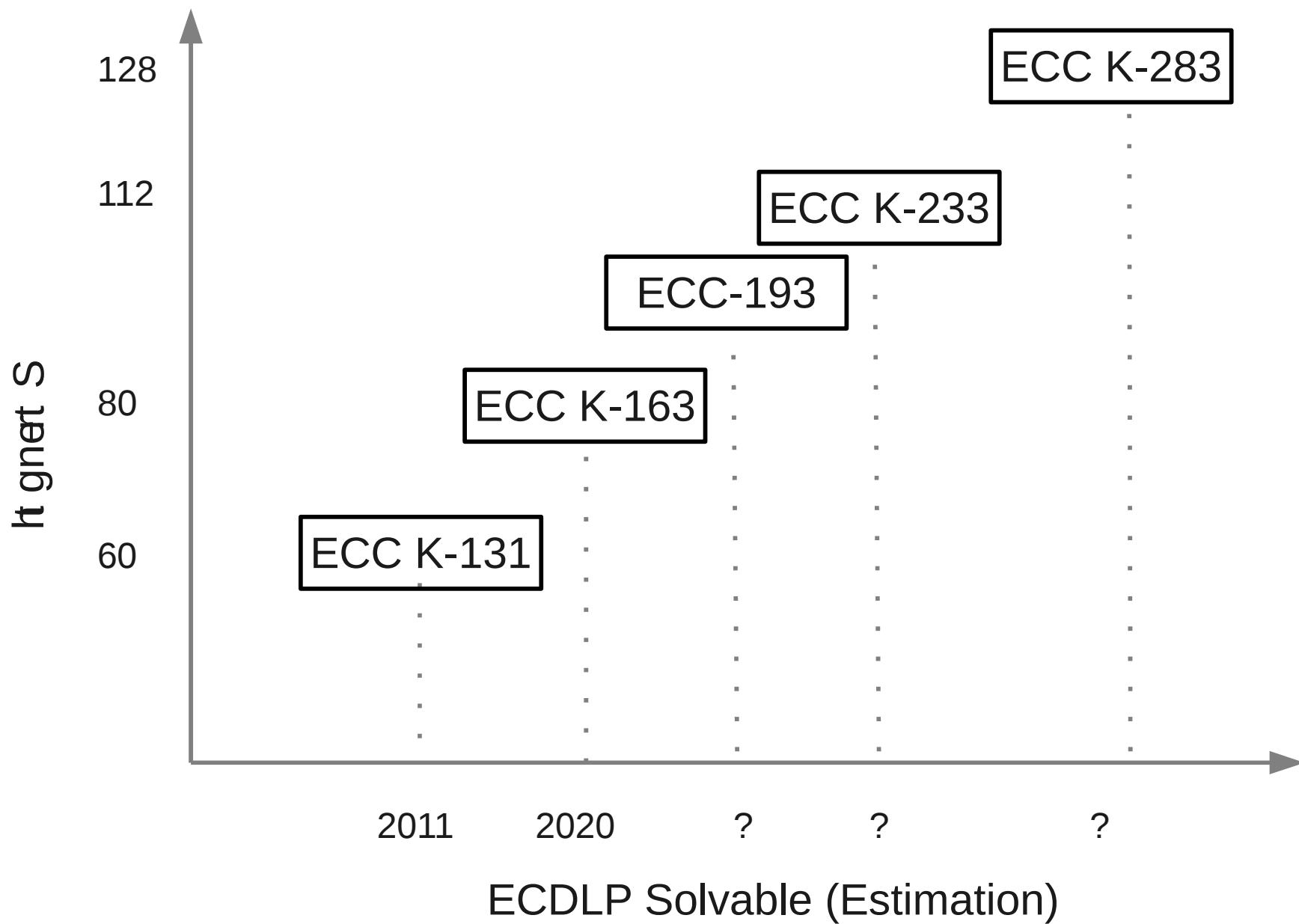


1-bit Add in  $\text{GF}(2^m)$

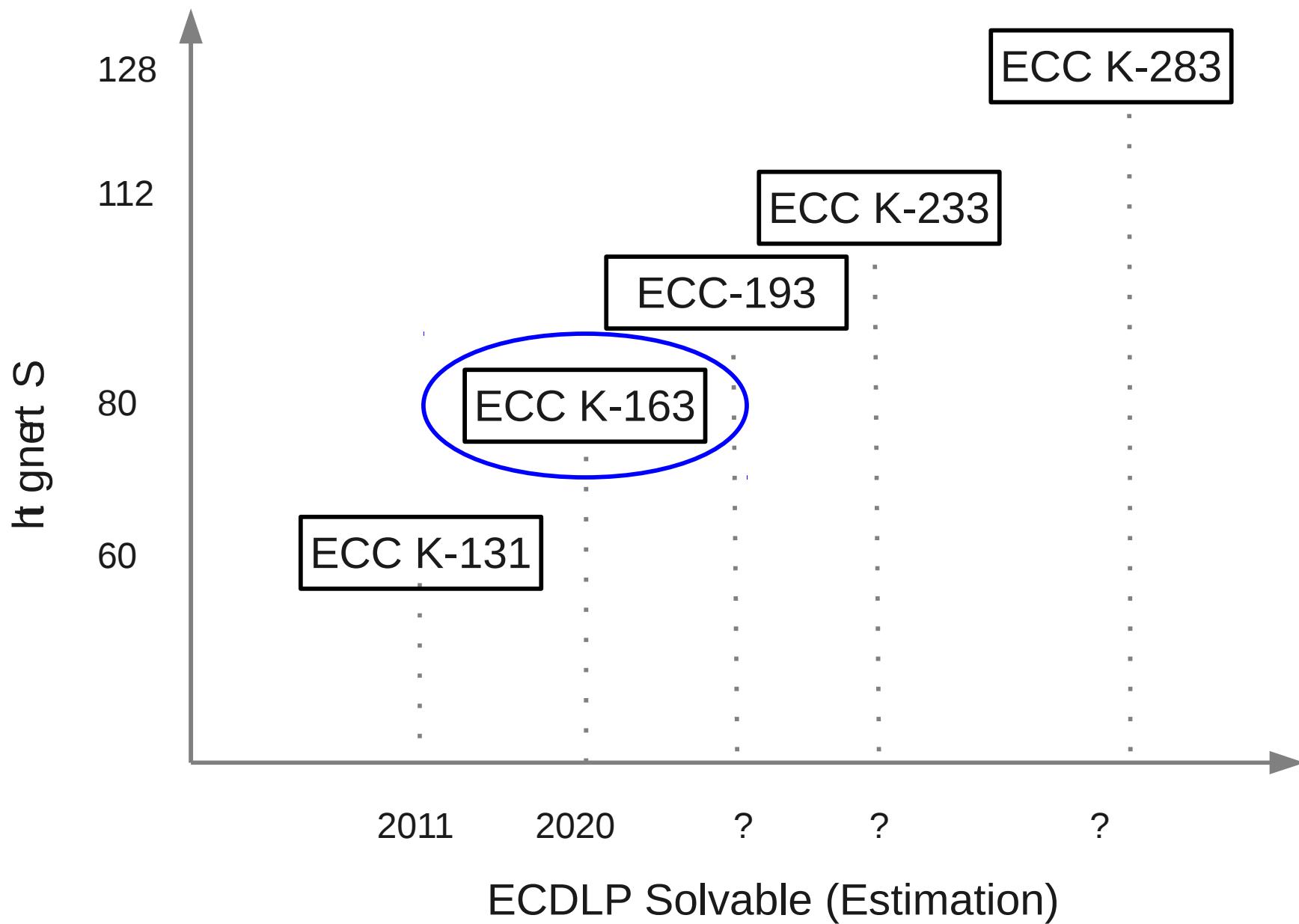


1-bit full-adder

## ➤ Security level



## ➤ Security level



## ➤ Coordinate systems

Coordinates	Point Representation	Inversion	Point Multiplication
Affine	$P_1=(x_1, y_1)$ $P_2=(x_2, y_2)$	Each key bit	-
Projective	$P_1=(X_1, Y_1, Z_1)$ $P_2=(X_2, Y_2, Z_2)$	One	-
López-Dahab (Affine)	$P_1=(x_1)$ $P_2=(x_2)$	Each key bit	Montgomery Ladder ( $P_2 = P_1 + P$ )
López-Dahab (Projective)	$P_1=(X_1, Z_1)$ $P_2=(X_2, Z_2)$	One	
* W-coordinate (Affine)	$P_1=(w_1)$ $P_2=(w_2)$	Each key bit	Montgomery Ladder ( $P_2 = P_1 + P$ )
* W-coordinate (Projective)	$P_1=(W_1, Z_1)$ $P_2=(W_2, Z_2)$	One	

\* Binary Edwards Curve only

## ➤ Coordinate systems

Coordinates	Point Representation	Inversion	Point Multiplication
Affine	$P_1=(x_1, y_1)$ $P_2=(x_2, y_2)$	Each key bit	-
Projective	$P_1=(X_1, Y_1, Z_1)$ $P_2=(X_2, Y_2, Z_2)$	One	-
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\* Binary Edwards Curve only

# › Count the number of registers

---

## Algorithm 1: Montgomery Powering Ladder

---

**Input:**  $k=\{1, k_{t-1}, \dots, k_0\}$  and point  $\mathbf{P}$

**Output:**  $[k]\mathbf{P}$

1:  $\mathbf{P}_1 \leftarrow \mathbf{P}$ ,  $\mathbf{P}_2 \leftarrow [2]\mathbf{P}$

2: for  $i=t-1$  to 0 do

3:   if  $k_i=1$  then

$\mathbf{P}_1 \leftarrow \mathbf{P}_1 + \mathbf{P}_2$ ,  $\mathbf{P}_2 \leftarrow [2]\mathbf{P}_2$

    else

$\mathbf{P}_2 \leftarrow \mathbf{P}_1 + \mathbf{P}_2$ ,  $\mathbf{P}_1 \leftarrow [2]\mathbf{P}_1$

4: end for

**Return**  $\mathbf{P}_1$

---

**Point Addition:**  
 $(X_1, Z_1) + (X_2, Z_2)$

$$\begin{aligned} T_1 &\leftarrow X_0 \\ X_1 &\leftarrow X_1 \cdot X_2 \\ Z_1 &\leftarrow Z_1 \cdot X_2 \\ T_2 &\leftarrow X_1 \cdot Z_1 \\ Z_1 &\leftarrow X_1 + Z_1 \\ Z_1 &\leftarrow Z_1^2 \\ X_1 &\leftarrow T_1 \cdot Z_1 \\ X_1 &\leftarrow X_1 + T_2 \end{aligned}$$


---

**Register:** 7  
**Mul.** : 4  
**Sqr.** : 1

**Point Doubling:**  
 $2(X_1, Z_1)$

$$\begin{aligned} T_1 &\leftarrow c \\ X_1 &\leftarrow X_1^2 \\ Z_1 &\leftarrow Z_1^2 \\ T_1 &\leftarrow Z_1 \cdot T_1 \\ Z_1 &\leftarrow X_1 \cdot Z_1 \\ T_1 &\leftarrow T_1^2 \\ X_1 &\leftarrow X_1^2 \\ X_1 &\leftarrow X_1 + T_1 \end{aligned}$$


---

**Register:** 3  
**Mul.** : 2  
**Sqr.** : 4

## › Common-Z trick ( $7 \rightarrow 6$ )

- 7 registers in total:

$(x_0, X_1, Z_1, X_2, Z_2, T_1, T_2)$

- Further reduction:

$(x_0, X_1, X_2, Z, T_1, T_2)$

$$X_1 \leftarrow X_1 \cdot Z_2$$

$$X_2 \leftarrow X_2 \cdot Z_1$$

$$Z \leftarrow Z_1 \cdot Z_2$$

- Cost for one iteration:

$$6M+5S \rightarrow 7M+4S$$

**Point Addition:**  
 $(X_1, Z_1) + (X_2, Z_2)$

$$\begin{aligned} T_1 &\leftarrow x_0 \\ X_1 &\leftarrow X_1 \cdot X_2 \\ Z_1 &\leftarrow Z_1 \cdot X_2 \\ T_2 &\leftarrow X_1 \cdot Z_1 \\ Z_1 &\leftarrow X_1 + Z_1 \\ Z_1 &\leftarrow Z_1^2 \\ X_1 &\leftarrow T_1 \cdot Z_1 \\ X_1 &\leftarrow X_1 + T_2 \end{aligned}$$

**Point Doubling:**  
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**Register:** 7

Mul. : 4

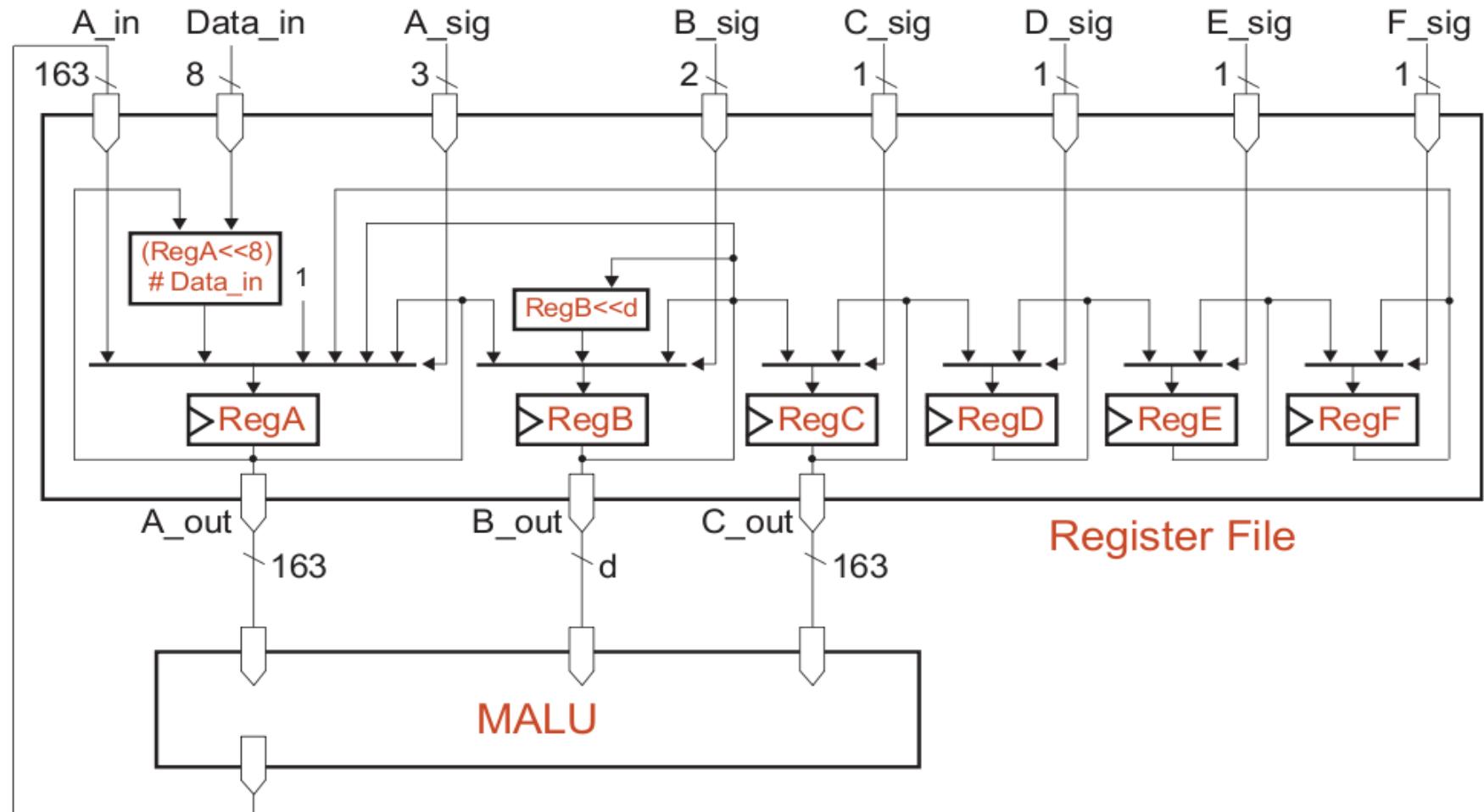
Sqr. : 1

**Register:** 3

Mul. : 2

Sqr. : 4

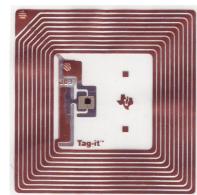
## ➤ Circular-shift register file



➤ Power & Energy

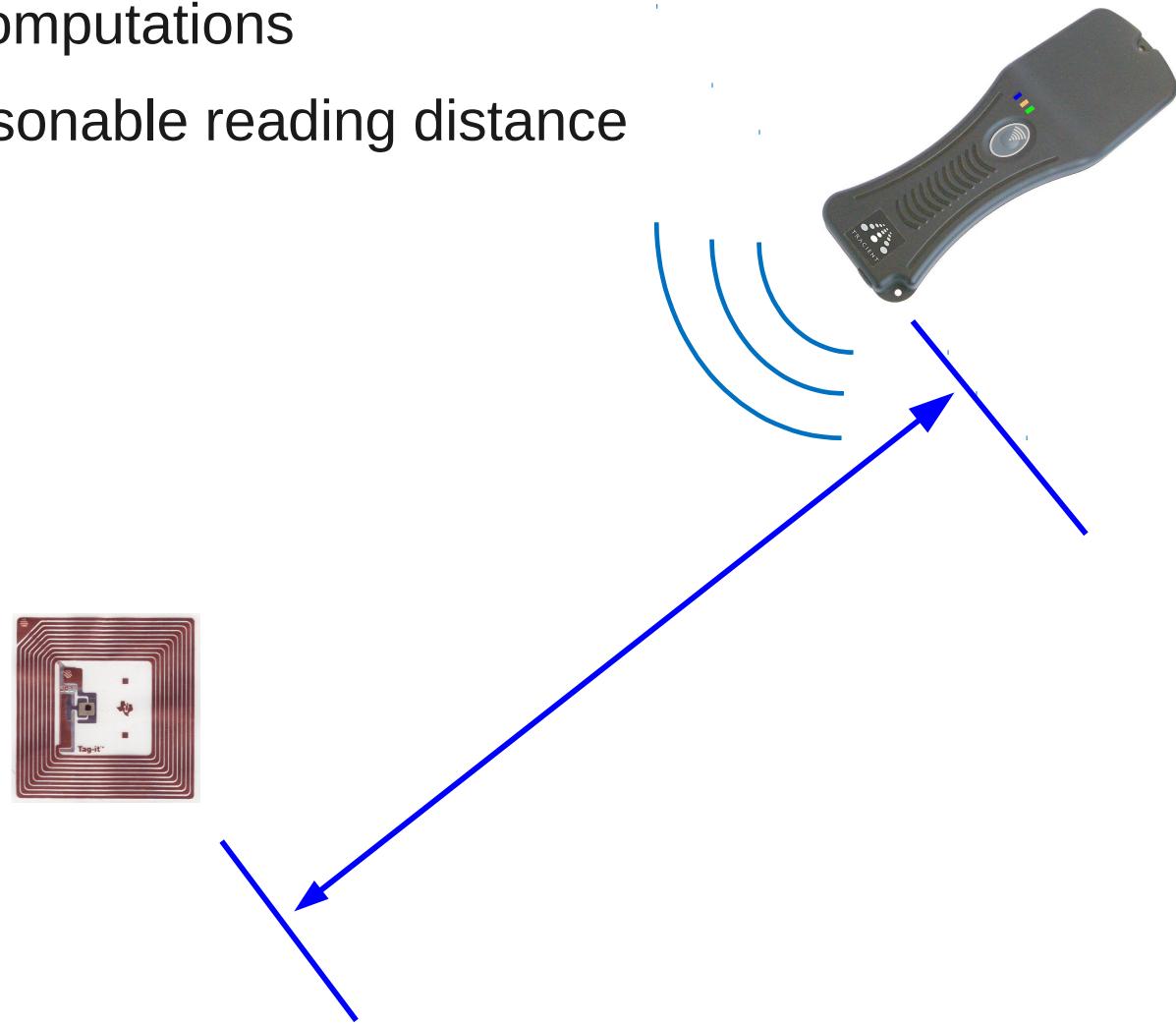
## ➤ Power & Energy

- To support the computations

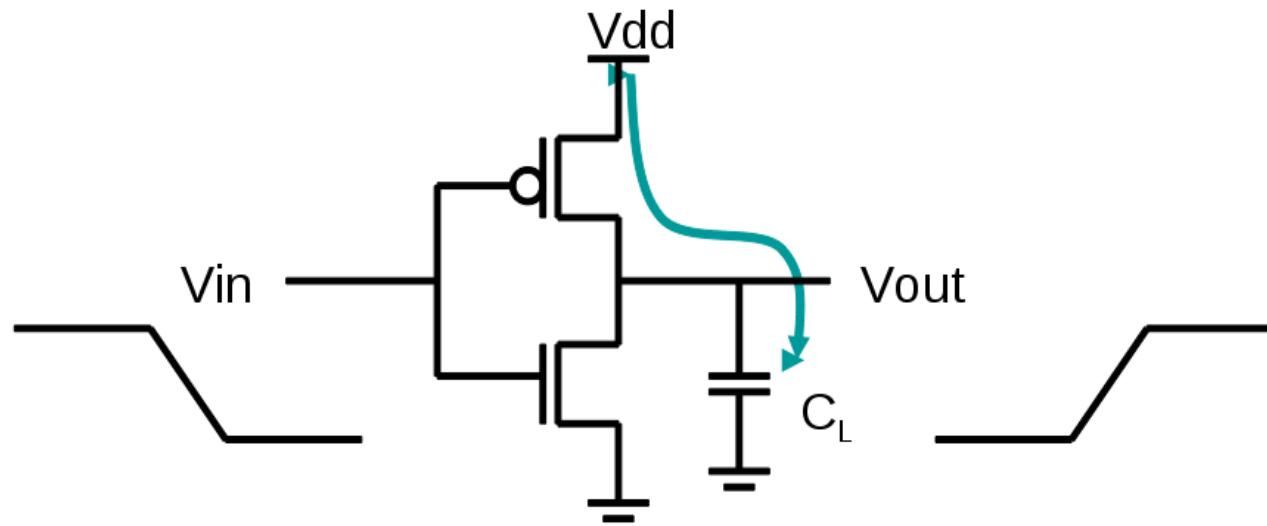


## ➤ Power & Energy

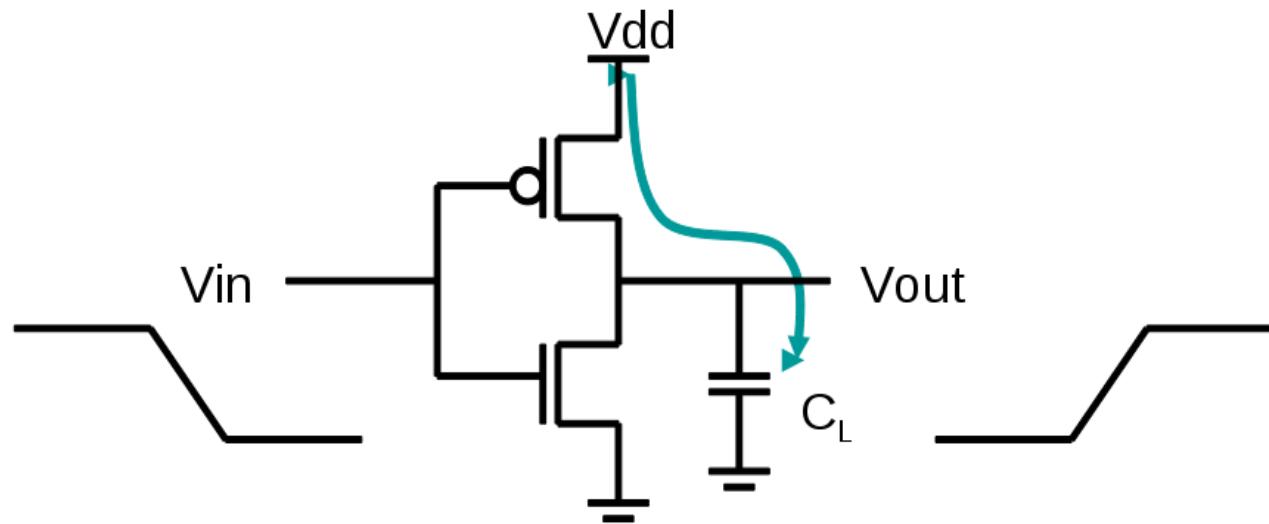
- To support the computations
- To support a reasonable reading distance



## ➤ Power & Energy



## ➤ Power & Energy



$$P_d = \alpha C V^2 f$$

Dynamic Power      Switch Activity      Output capacitance       $V_{dd}$       Clock Frequency

The equation  $P_d = \alpha C V^2 f$  is shown with arrows pointing from each term to its corresponding label below the equation. The term  $\alpha$  is labeled "Switch Activity",  $C$  is labeled "Output capacitance",  $V^2$  is labeled " $V_{dd}$ ", and  $f$  is labeled "Clock Frequency". The term  $\alpha$  is also labeled "Dynamic Power".

## › A bit-serial multiplier

---

**Input:**  $A(x) = \{a_{m-1}, a_{m-2} \dots a_1, a_0\}$ ,

$B(x) = \{b_{m-1}, b_{m-2} \dots b_1, b_0\}$ ,

and  $P(x) = \{1, p_{m-1} \dots p_1, 1\}$

**Output:**  $C(x) = A(x)B(x) \bmod P(x)$

---

1:  $C(x) \leftarrow 0$ ;

2: **for**  $i = m-1$  to 0 **do**

3:  $C(x) \leftarrow xC(x) + b_i A(x)$ ;

$C(x) \leftarrow C(x) \bmod P(x)$ ;

4: **end for**

**Return:**  $C(x)$

---

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$B(x) = \{b_{m-1}, b_{m-2} \dots b_1, b_0\}$ ,

and  $P(x) = \{1, p_{m-1} \dots p_1, 1\}$

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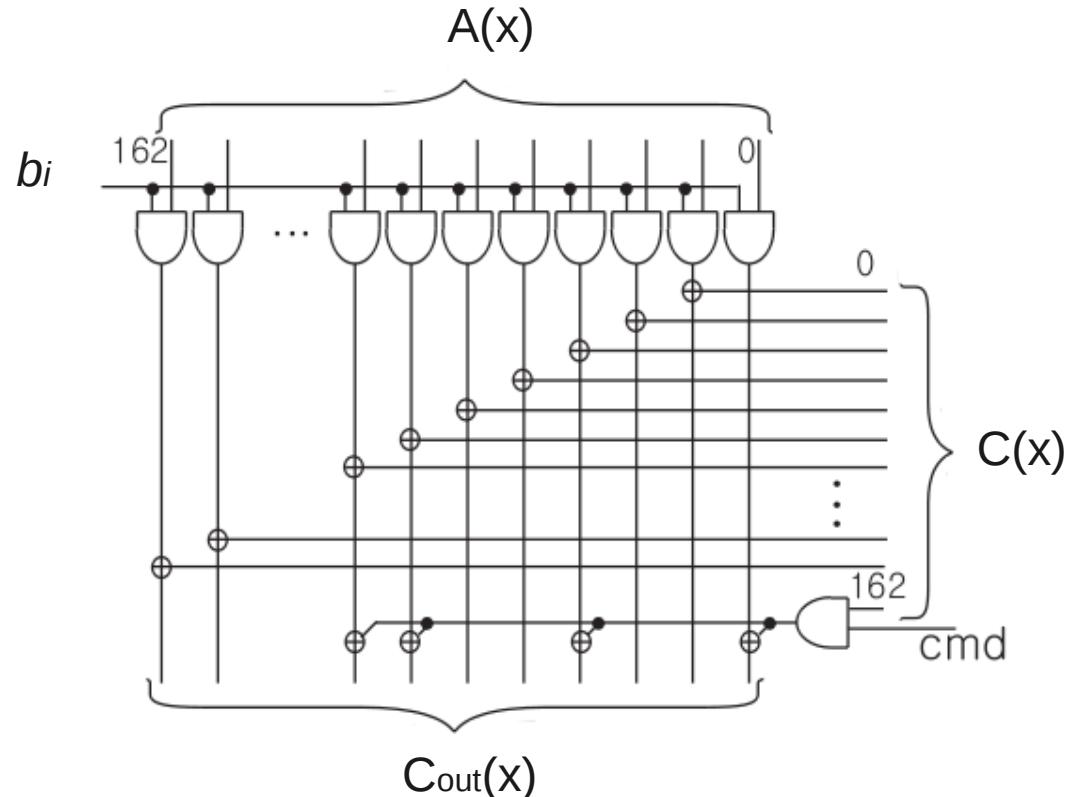
2: **for**  $i = m-1$  to 0 **do**

3:  $C(x) \leftarrow xC(x) + b_i A(x);$

$C(x) \leftarrow C(x) \bmod P(x);$

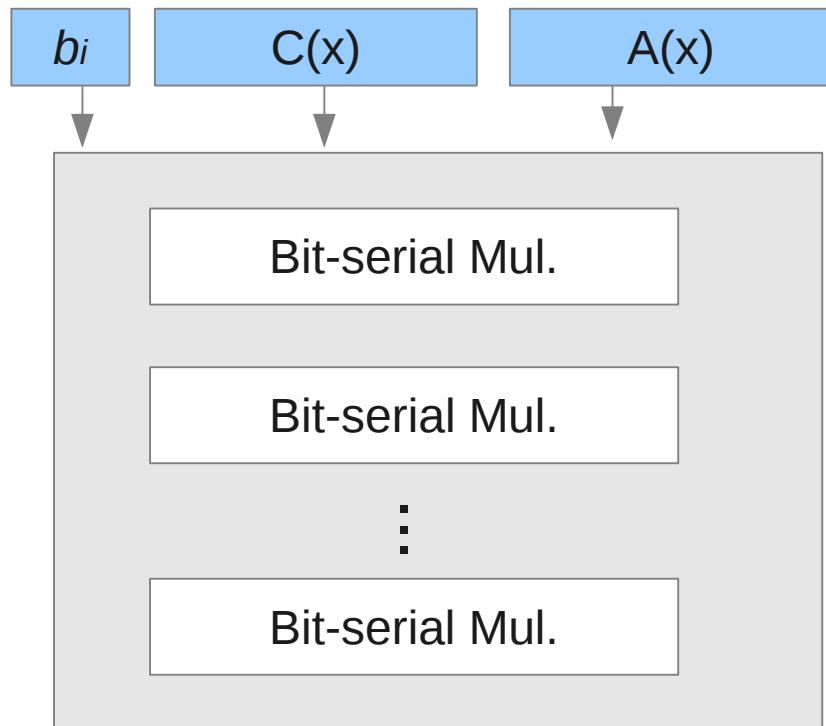
4: **end for**

**Return:**  $C(x)$

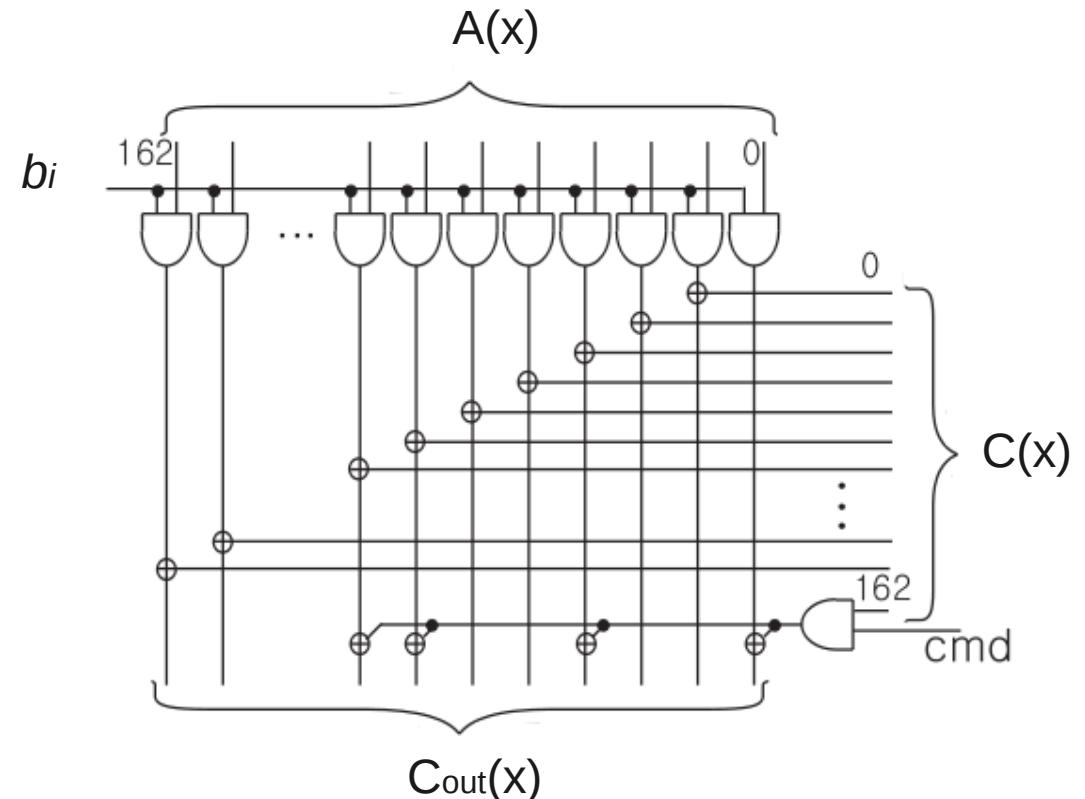


Bit-serial multiplier  
[ Delay:  $\approx m$  cycles ]

## ➤ Power & Energy



Digit-serial Multiplier  
[ Delay:  $\approx m/d$  cycles ]



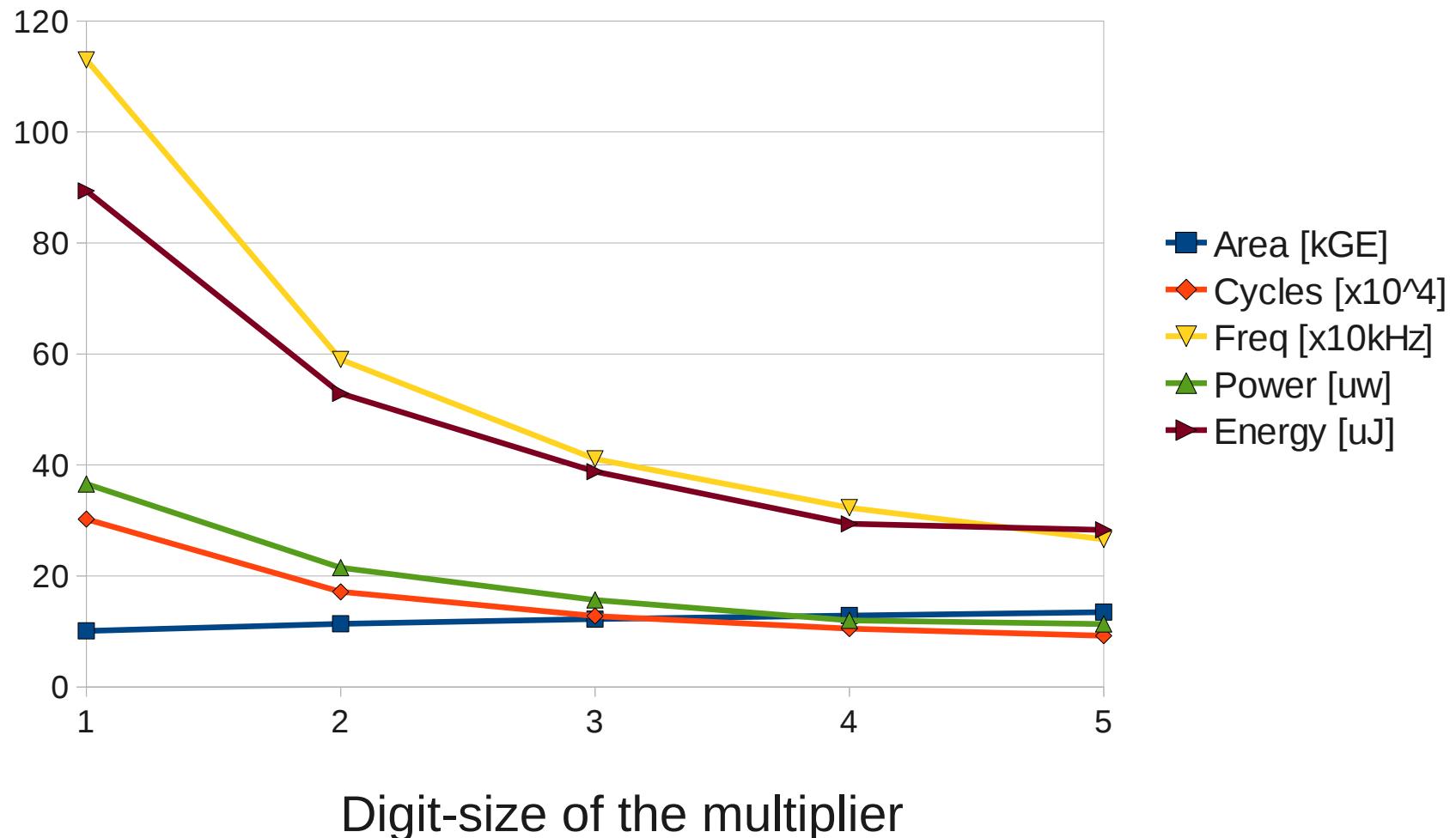
Bit-serial multiplier  
[ Delay:  $\approx m$  cycles ]

## ➤ Power & Energy

- Target : One point multiplication within 0.25s

## ➤ Power & Energy

- Target : One point multiplication within 0.25s



- Physical attacks

## ➤ Physical attacks

### Side-Channel Analysis



## ➤ Physical attacks

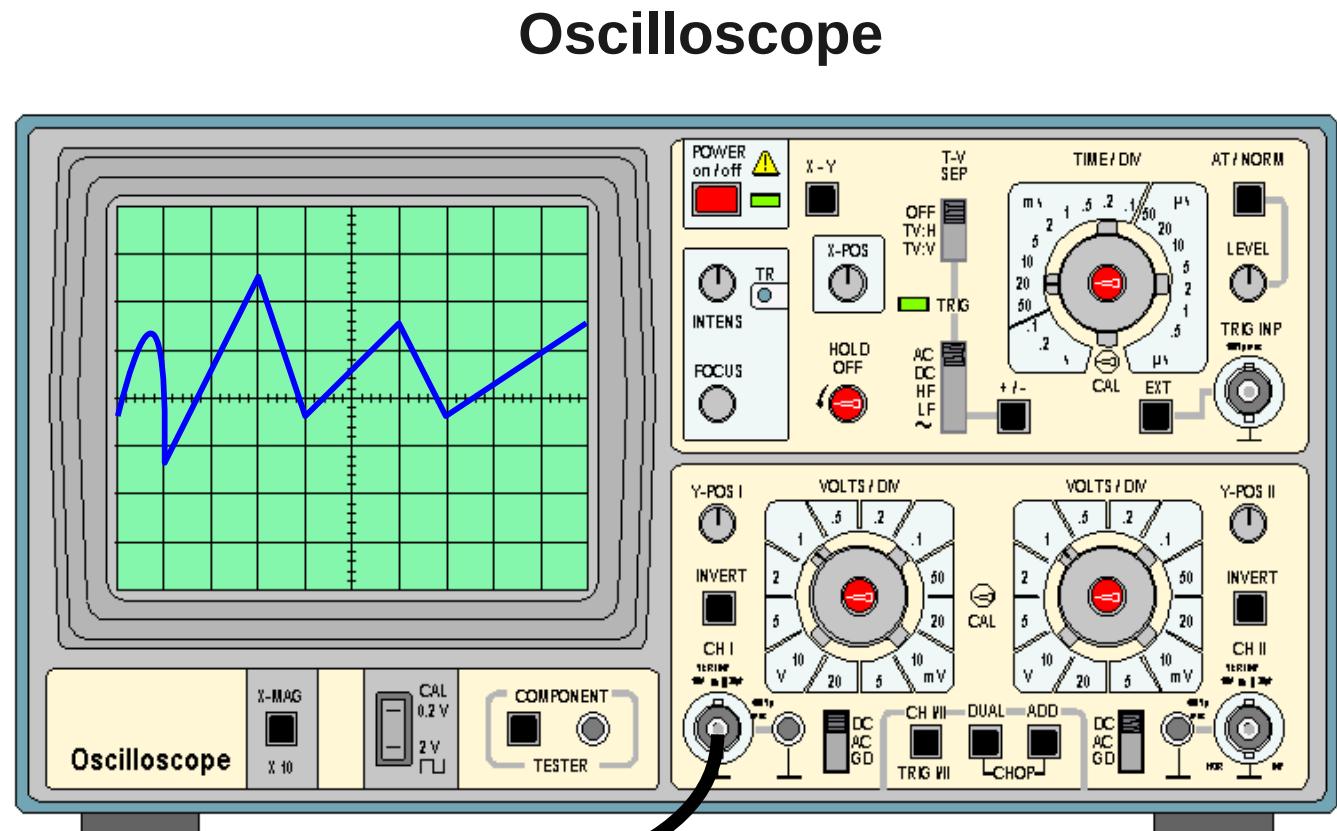
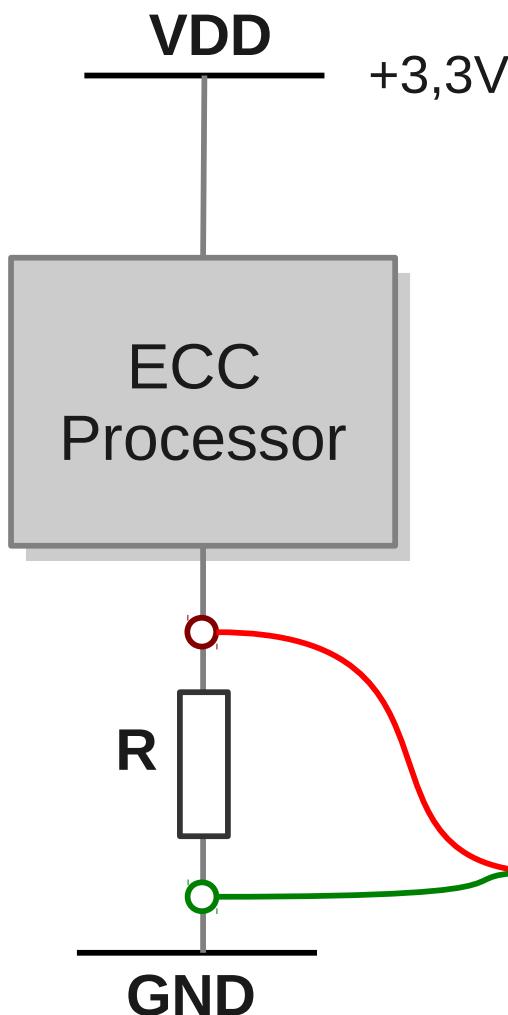
Side-Channel Analysis



Fault Analysis



## ➤ Power analysis



## ➤ Simple power analysis

$$\mathbf{k} = (k_{l-1}, k_{l-2}, \dots, k_0)$$

Left-to-right binary method for point multiplication

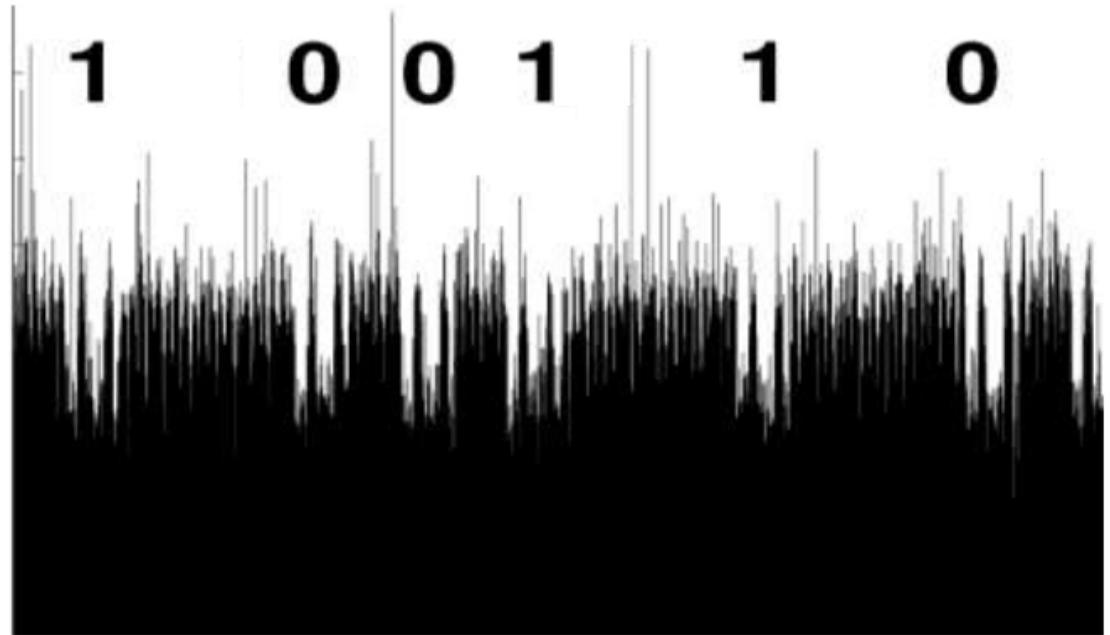
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R ← 0
for i=l-1 downto 0 do
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    if ki = 1 then
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end for
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## ➤ Montgomery Ladder?

---

### Algorithm 1: Montgomery Powering Ladder

---

**Input:**  $k=\{1, k_{t-1}, \dots, k_0\}$  and point  $\mathbf{P}$

**Output:**  $[k]\mathbf{P}$

1:  $\mathbf{P}_1 \leftarrow \mathbf{P}$ ,  $\mathbf{P}_2 \leftarrow [2]\mathbf{P}$

2: for  $i=t-1$  to 0 do

3:   if  $k_i=1$  then

$\mathbf{P}_1 \leftarrow \mathbf{P}_1 + \mathbf{P}_2$ ,  $\mathbf{P}_2 \leftarrow [2]\mathbf{P}_2$

    else

$\mathbf{P}_2 \leftarrow \mathbf{P}_1 + \mathbf{P}_2$ ,  $\mathbf{P}_1 \leftarrow [2]\mathbf{P}_1$

4: end for

**Return**  $\mathbf{P}_1$

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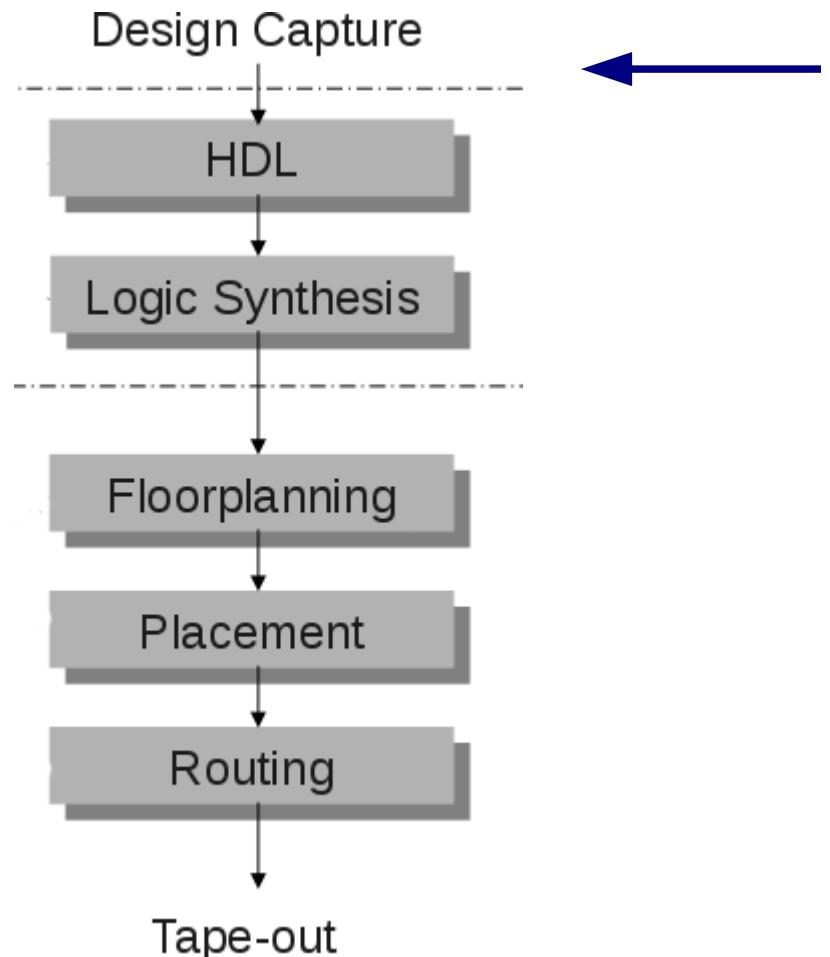
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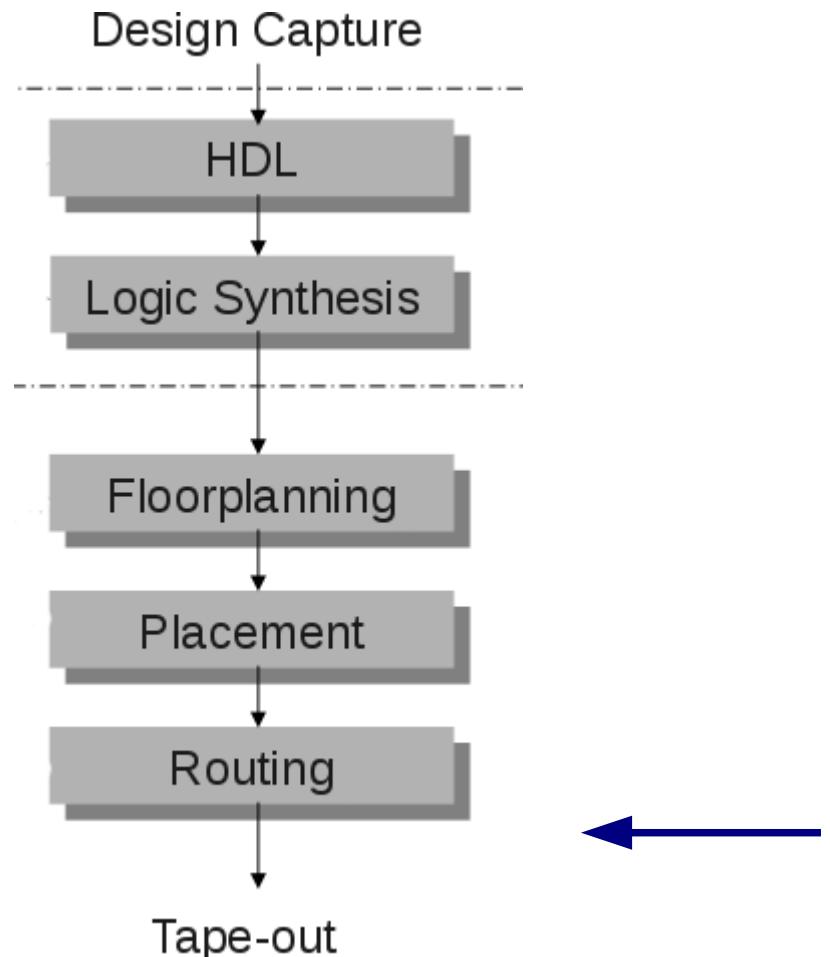
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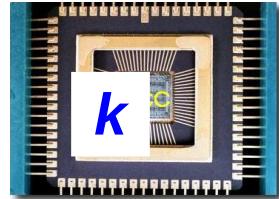
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---



- Differential power analysis

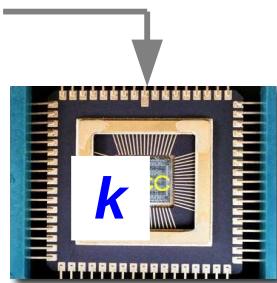
- Differential power analysis



Power  
Model

## ➤ Differential power analysis

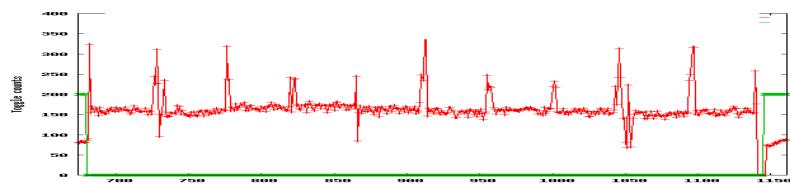
$P_1, P_2, \dots, P_n$



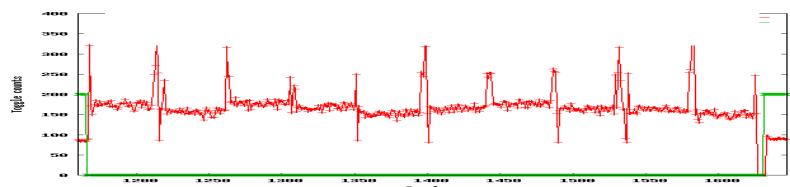
Power Model

$[k]P_1, [k]P_2, \dots, [k]P_n$

$[k]P_1$

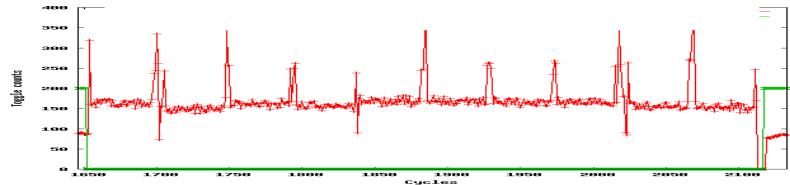


$[k]P_2$



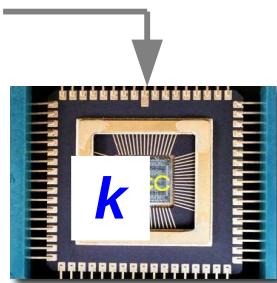
⋮

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## ➤ Differential power analysis

$P_1, P_2, \dots, P_n$

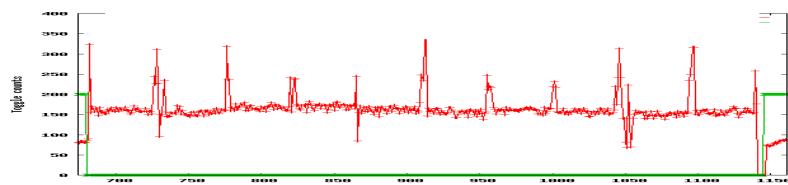


Key guess  $k=k'$

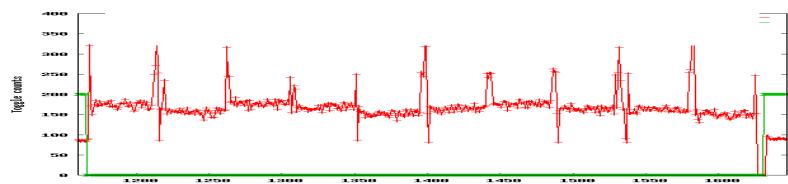
Power Model

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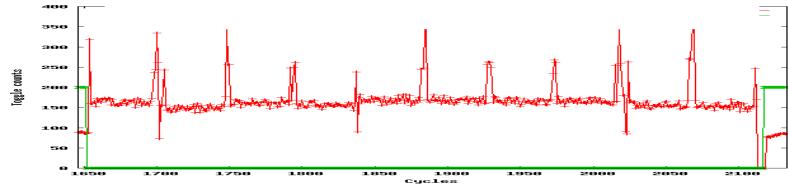


$[k]P_2$

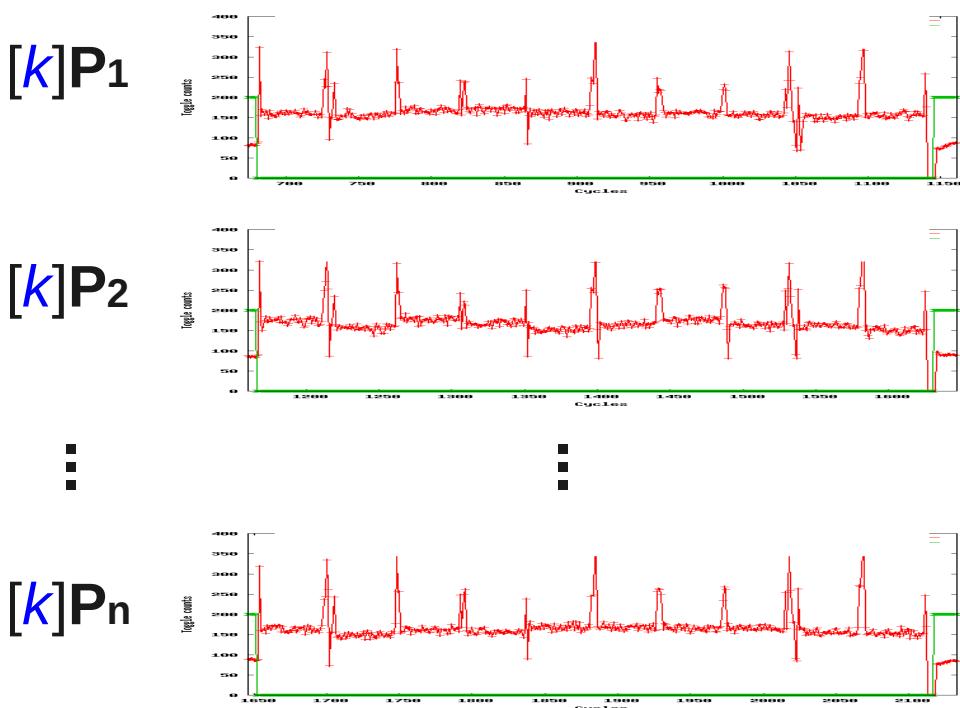
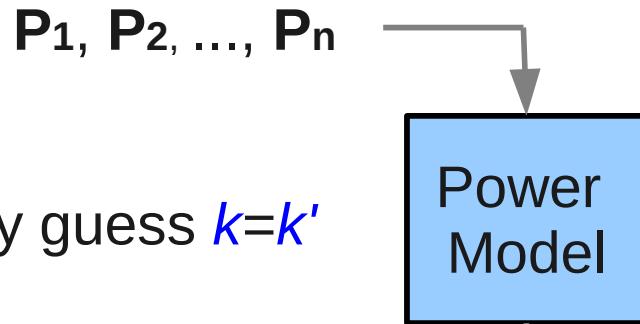
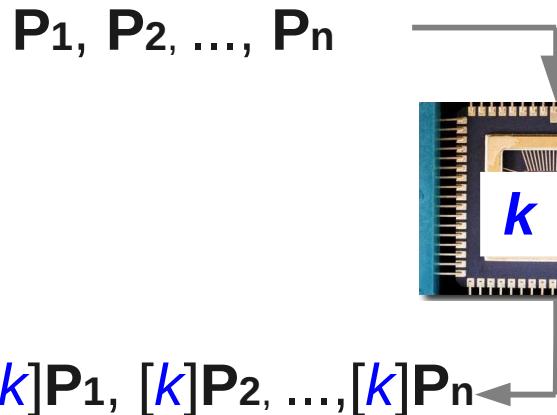


⋮

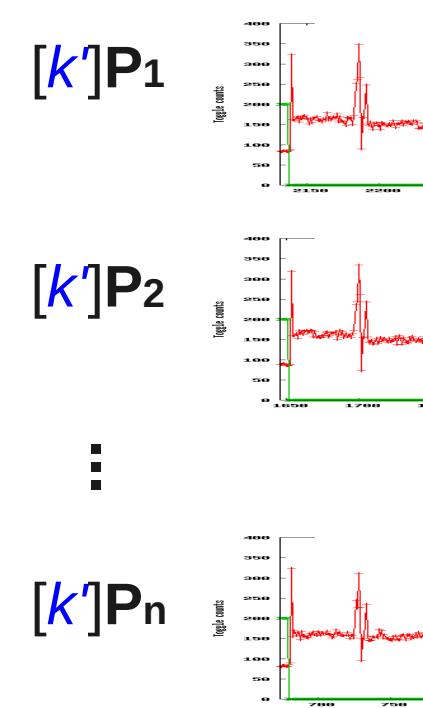
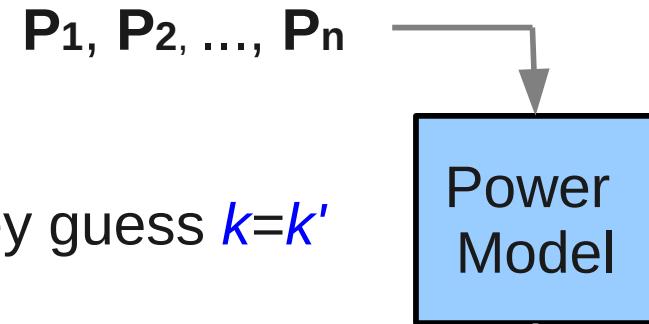
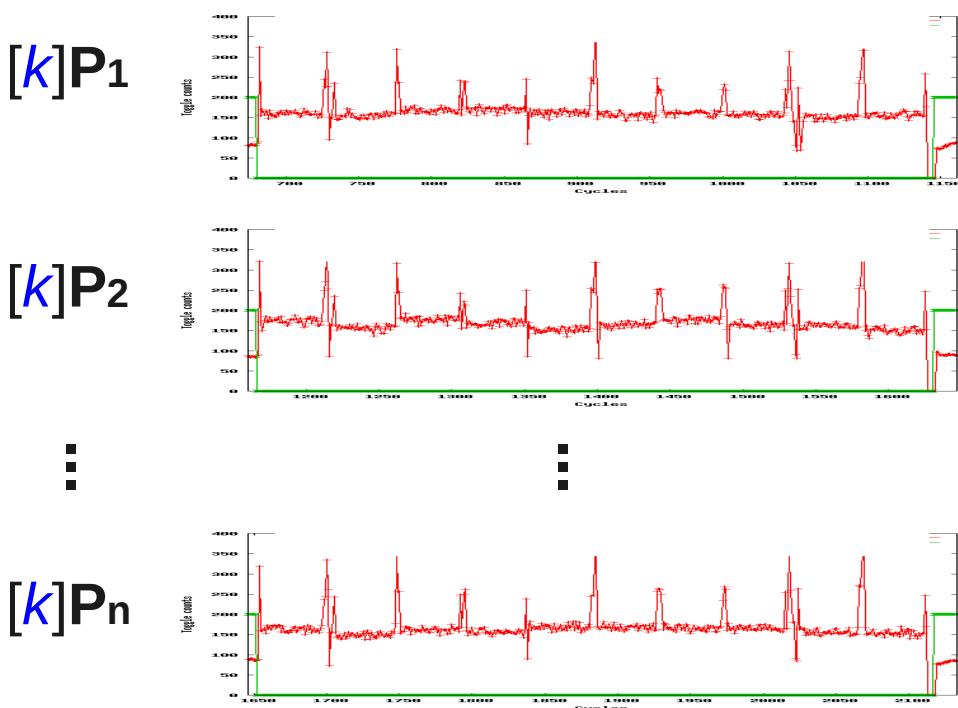
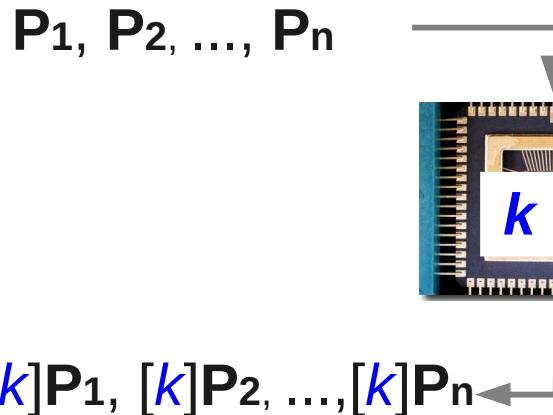
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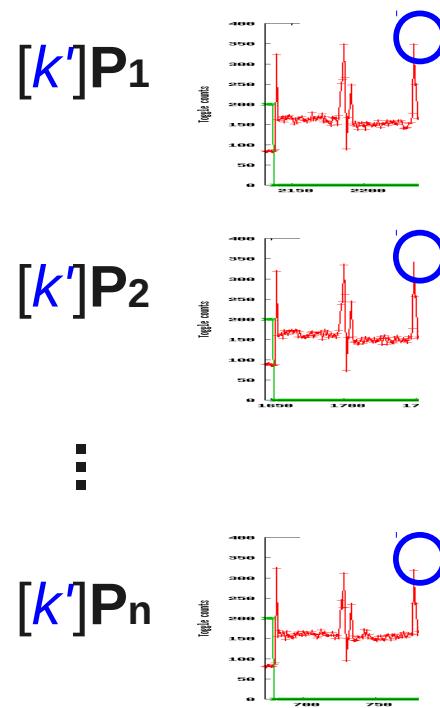
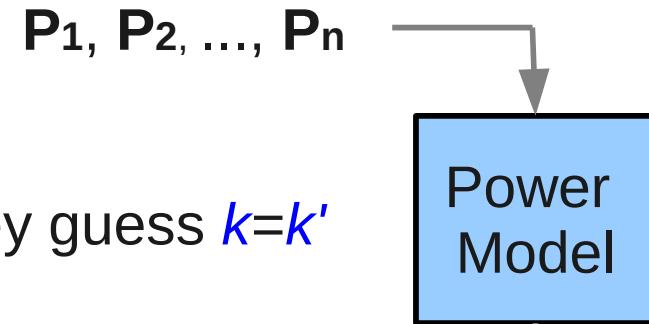
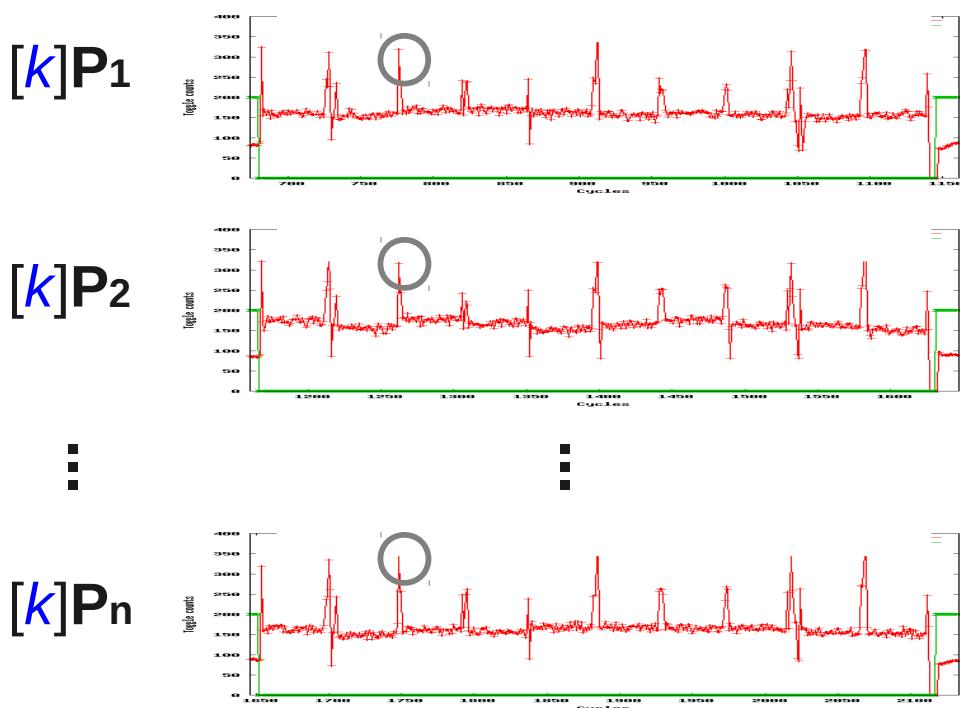
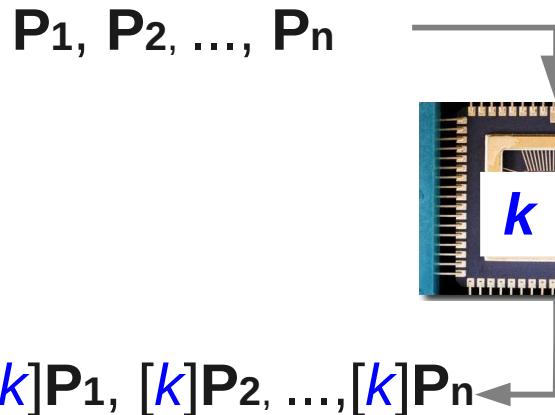
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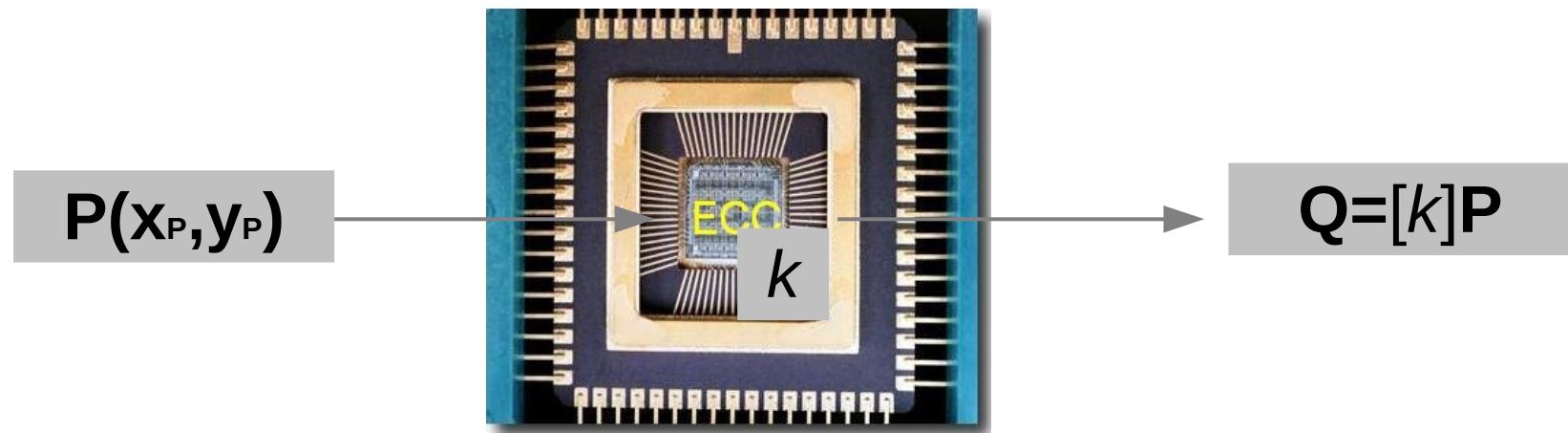


- Fault analysis

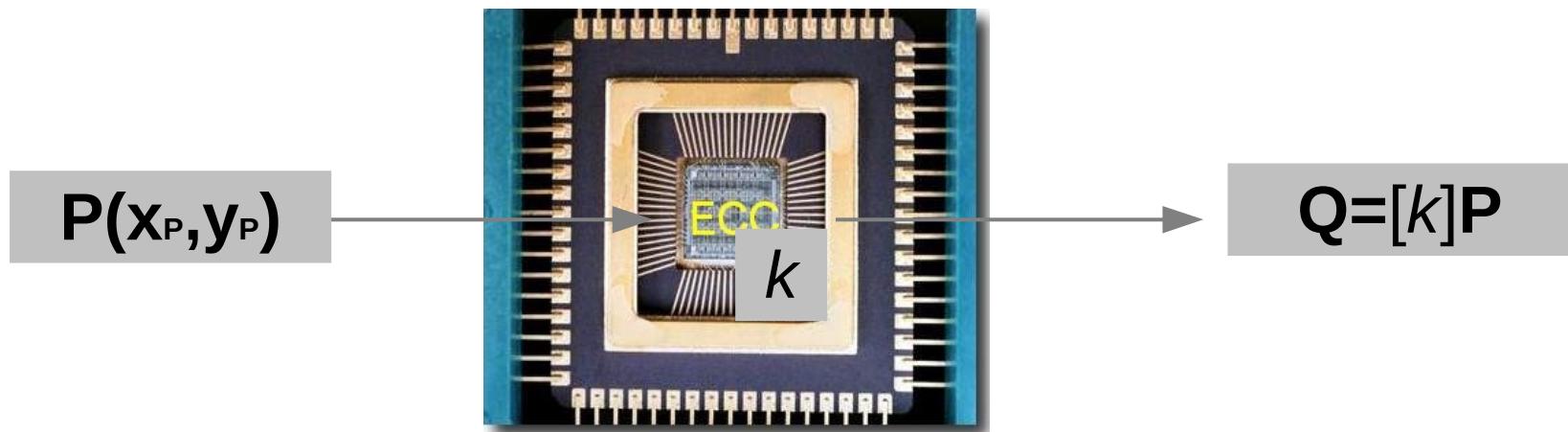
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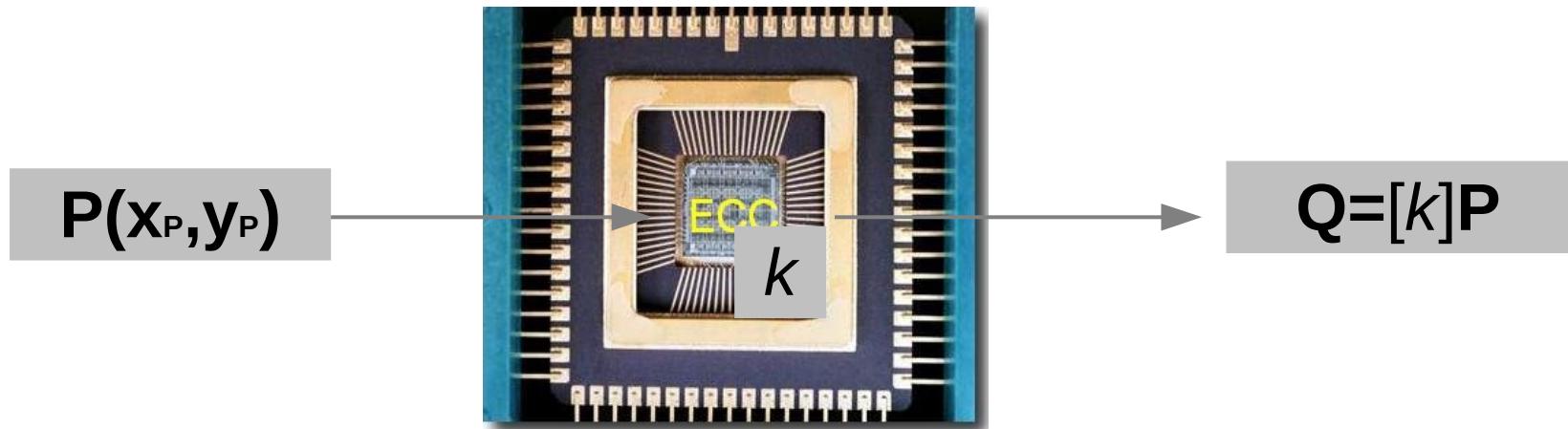


- The specified curve is:

$$E : y^2 + a_1 xy + a_3 y = x^3 + a_2 x^2 + a_4 x + a_6,$$

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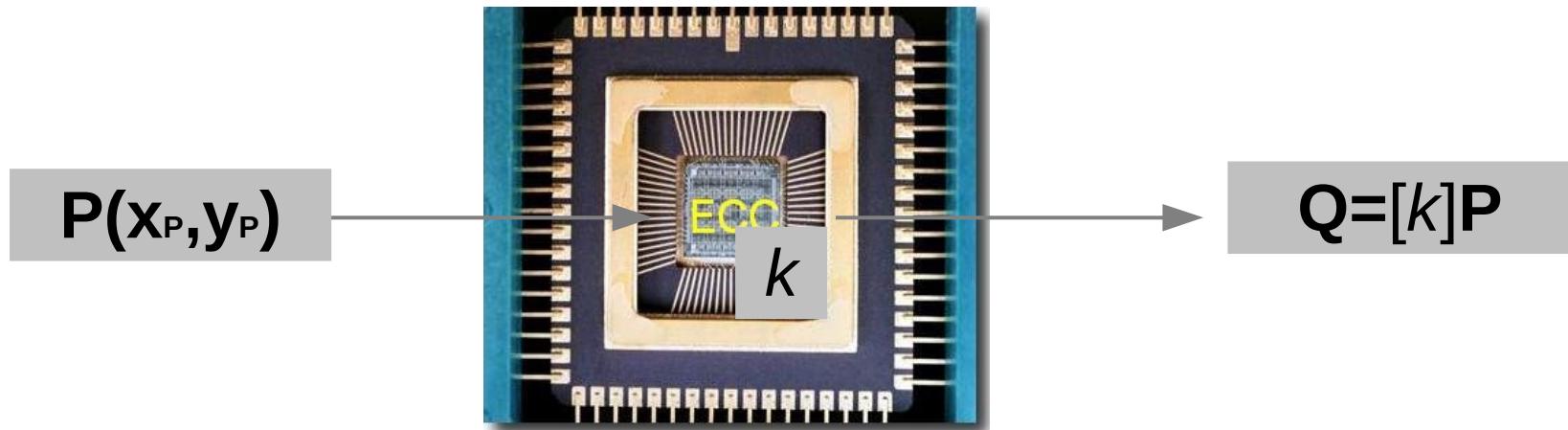
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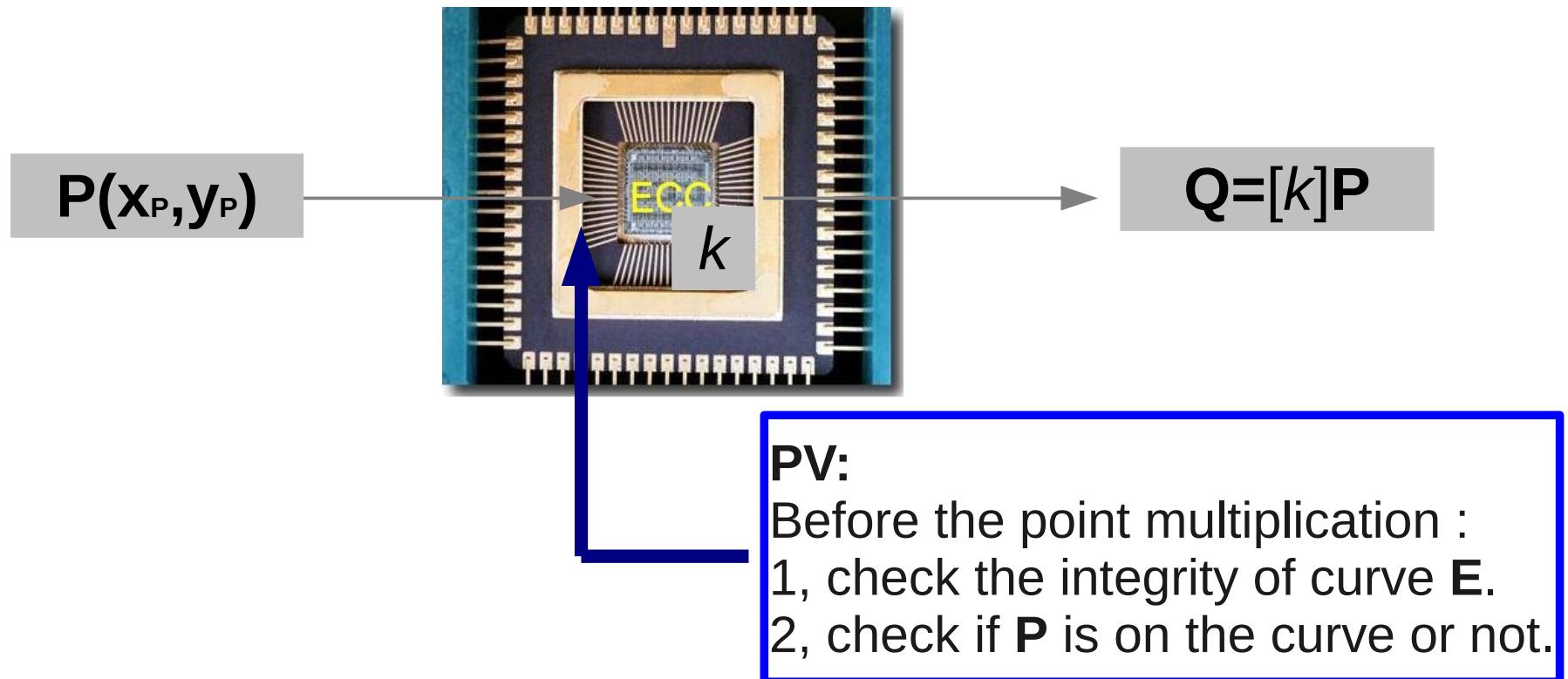
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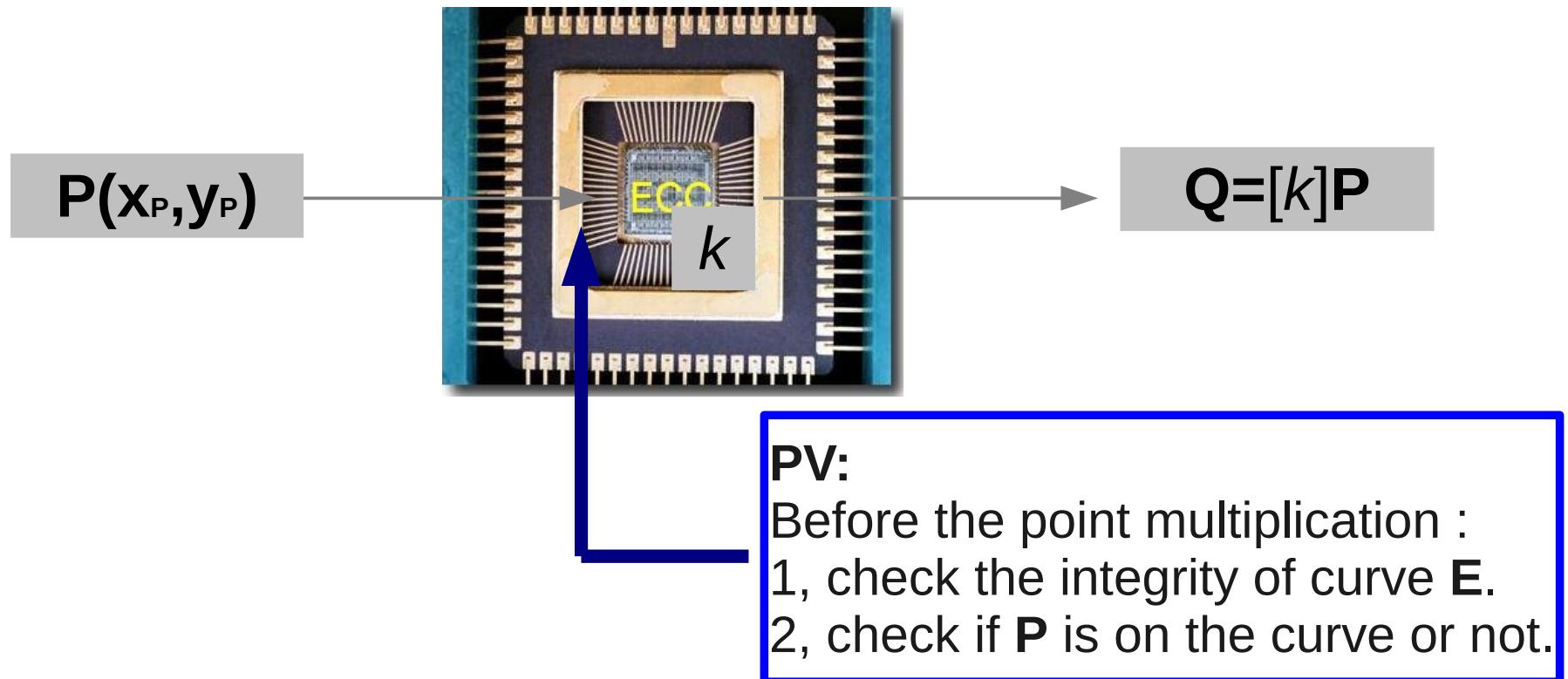
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Not used for PA/PD

## › Point validation



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**But:**

Can the adversary inject faults after the validation step?

➤ Fault analysis (twist curve) [Fouque+'08]

- Consider a curve defined on  $\mathbb{F}_p$ :

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✓: Effective    x: Attacked    -: Not related    H: helps the attack  
 ?: Not clear or not published    \*: Implementation dependent

	Passive attacks								Active attacks					
	SPA TA	Temp- late	DPA Attack	Doubl. Attack	RPA ZPA	Carry based	M type	C type	Safe-error Invalid Point	Weak curve Invalid curve	Twist curve	Sign change	Differential Fault	
Indistinguishable PA/PD	✓	-	-	?	-	-	-	-	-	-	-	-	-	-
Double-add-always	✓	-	-	x	-	-	-	H	-	-	-	-	-	-
Montgomery ladder $\perp$	✓	-	-	x	?	-	✓*	-	-	-	-	H	✓	-
Montgomery ladder $\top$	✓	-	-	x	x	-	✓*	-	-	-	-	✓	-	-
Random key splitting	-	?	✓	?	✓	x	-	-	-	-	-	?	?	?
Scalar randomization	-	x	x	x	✓	x	-	-	-	-	-	-	?	?
Base point blinding	-	x	x	x	✓	-	-	-	?	*?	-	-	-	?
Randomized proj. coord.	-	✓	✓	?	x	-	-	-	-	-	-	-	-	?
Randomized EC Iso.	-	?	✓	?	x	-	-	-	-	-	-	-	-	?
Randomized Field Iso.	-	?	✓	?	x	-	-	-	-	-	-	-	-	?
Point validity check	-	-	-	-	-	-	-	H	✓	?	✓ $\perp$	H	✓	
Curve integrity check	-	-	-	-	-	-	-	-	-	✓	-	-	-	
Coherence check	-	-	-	-	-	-	-	H	-	?	-	✓*	✓	

## › Attacking points

- Tag's private key:  $x$
- Tag's public key :  $X = [-x]P$

**Reader (Verifier)**

$r_2 = \text{TRNG}()$

If  $[v]P + [r_2]X == R_1$   
Then accept

$R_1$

$r_2$

$v$

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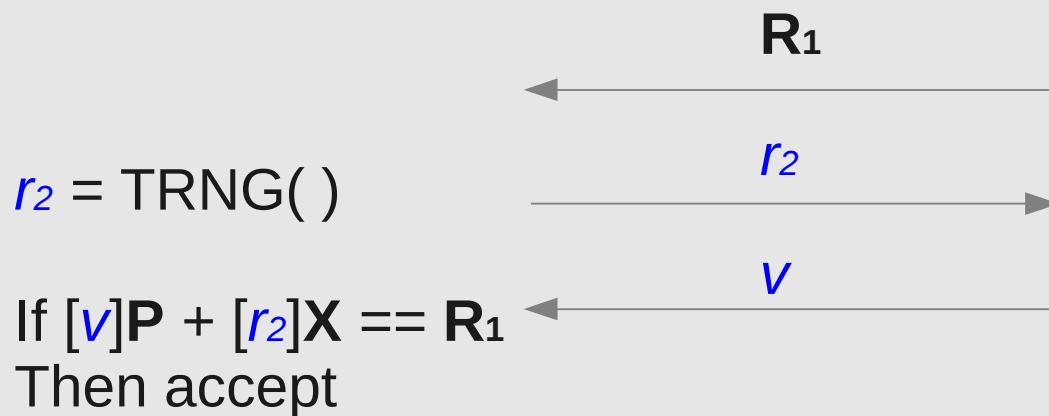


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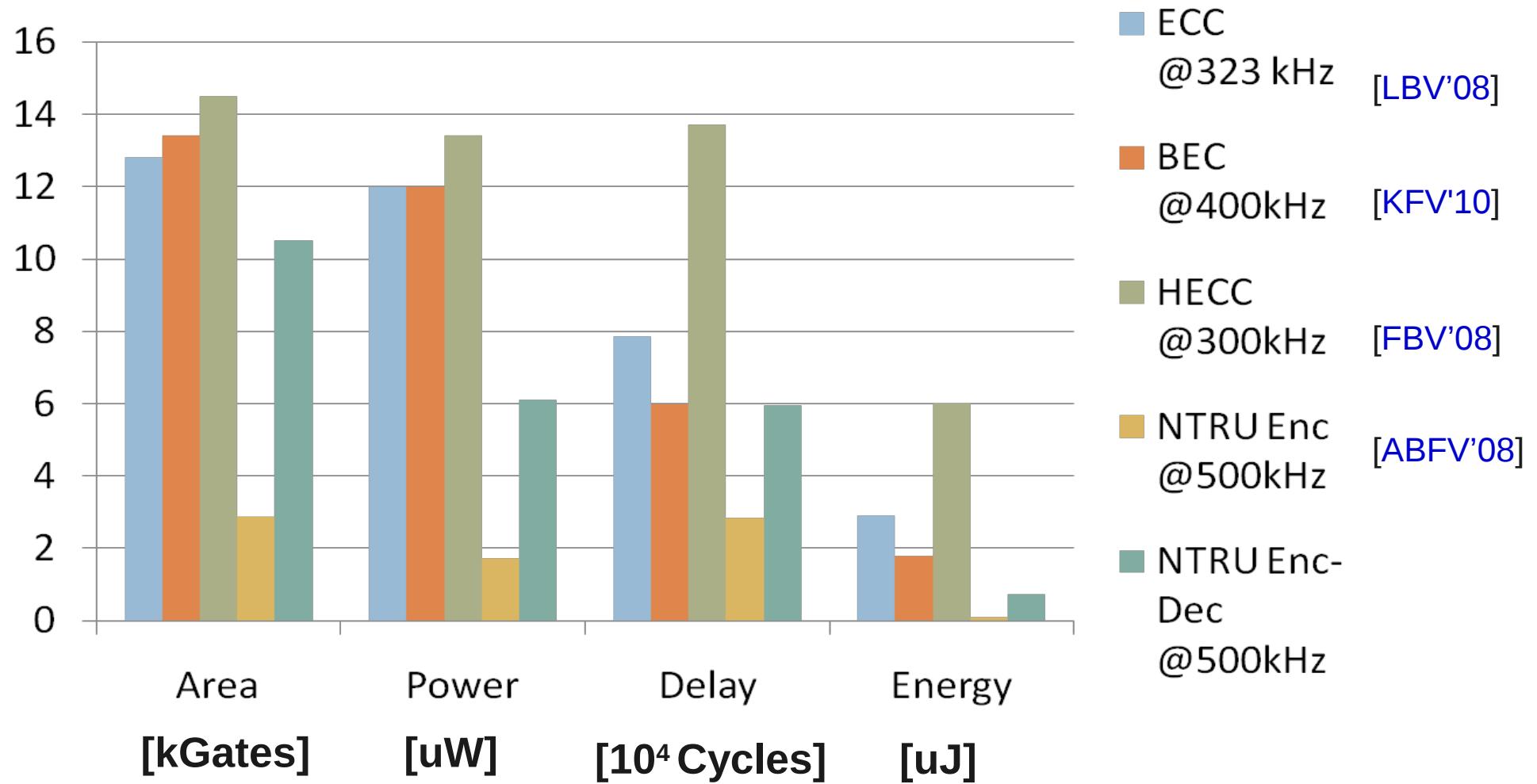
+

The protocol has minimum attacking points

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Lightweight countermeasures

## ➤ Comparison

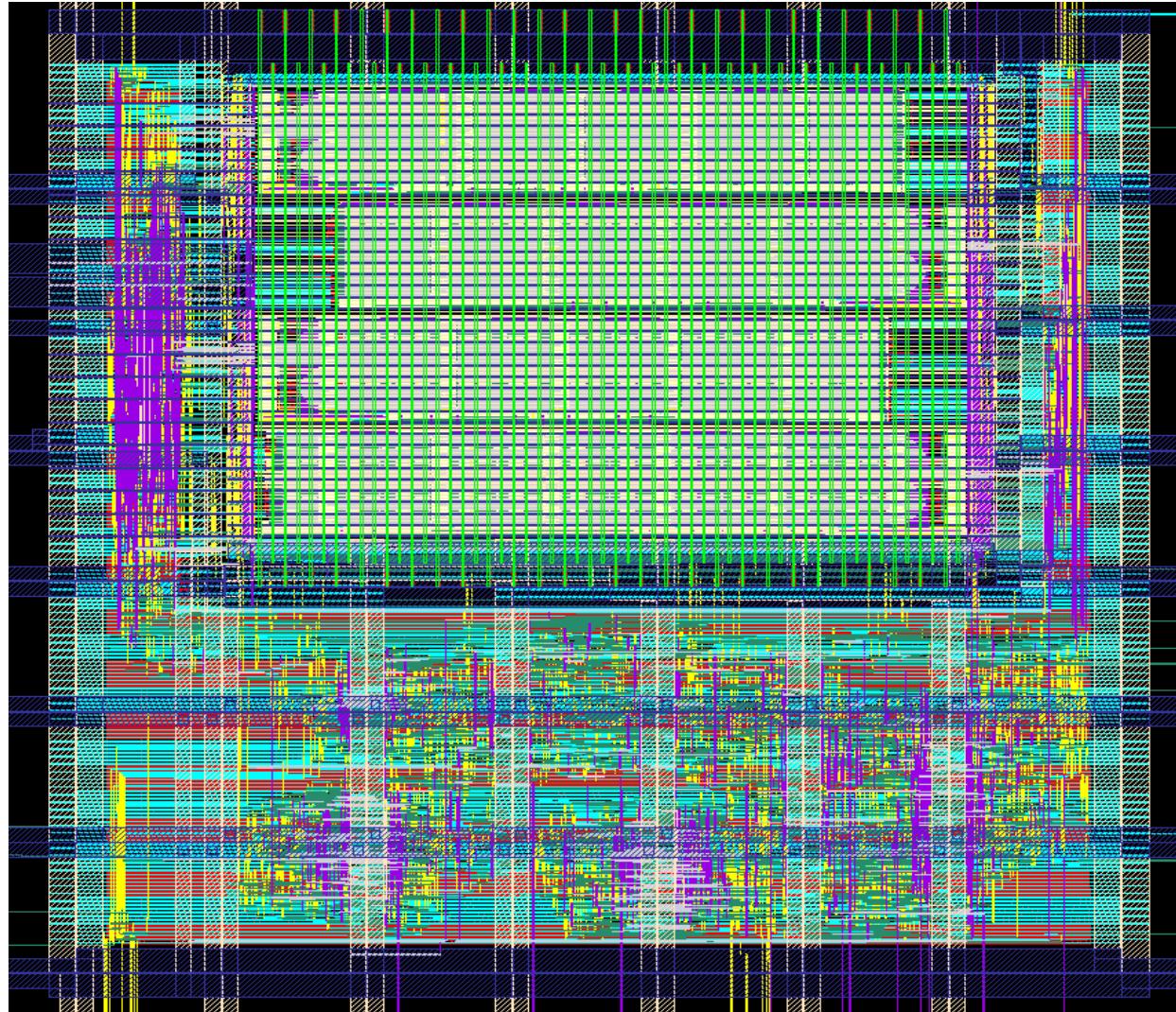


\* ECC/BEC over GF( $2^{163}$ )

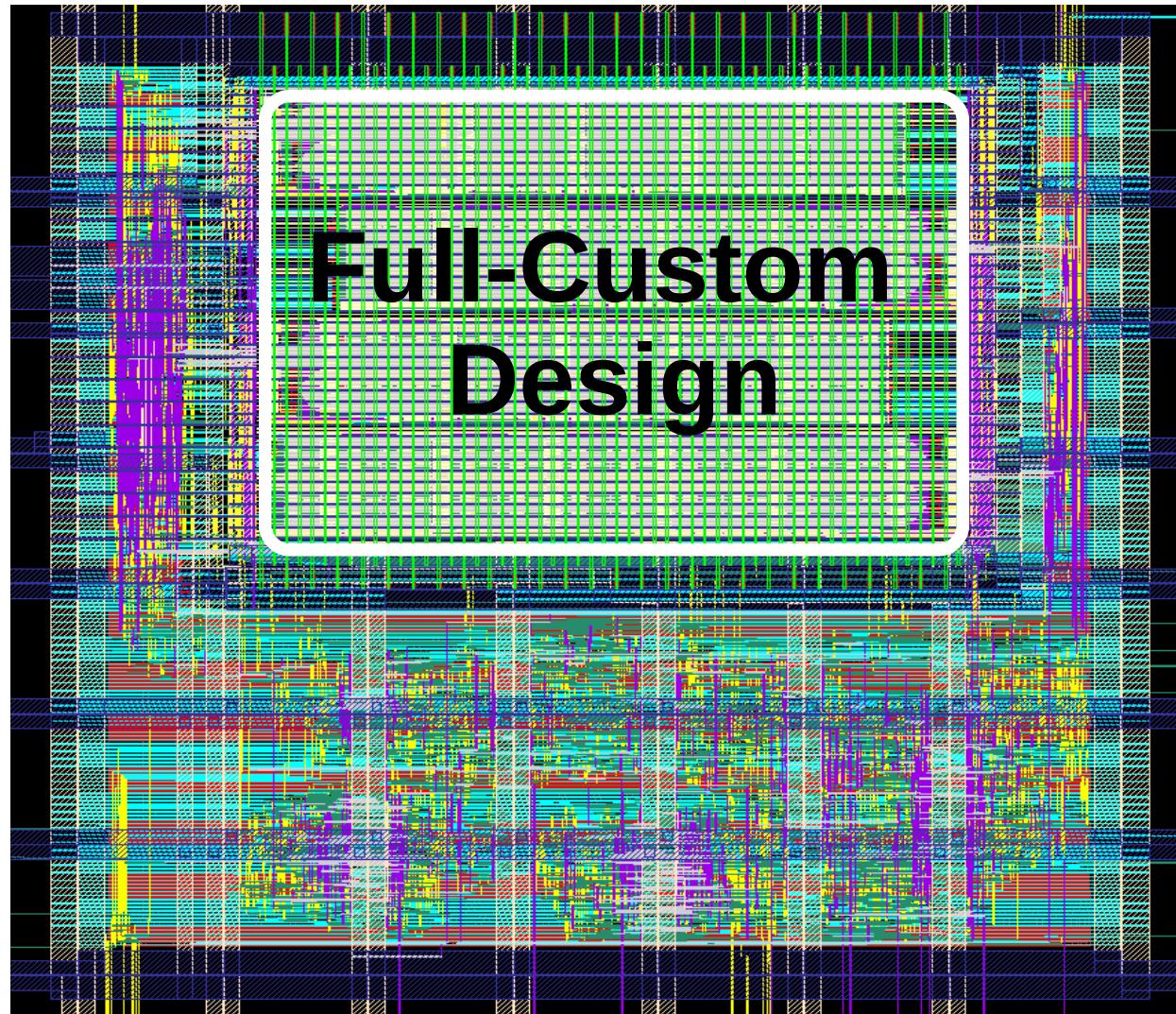
\* HECC over GF( $2^{83}$ )

\* NTRU parameter: {N=167, q=128, p=3}

- An ECC processor for RFID (Expected in Nov, 2010)



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Thanks for your attention.